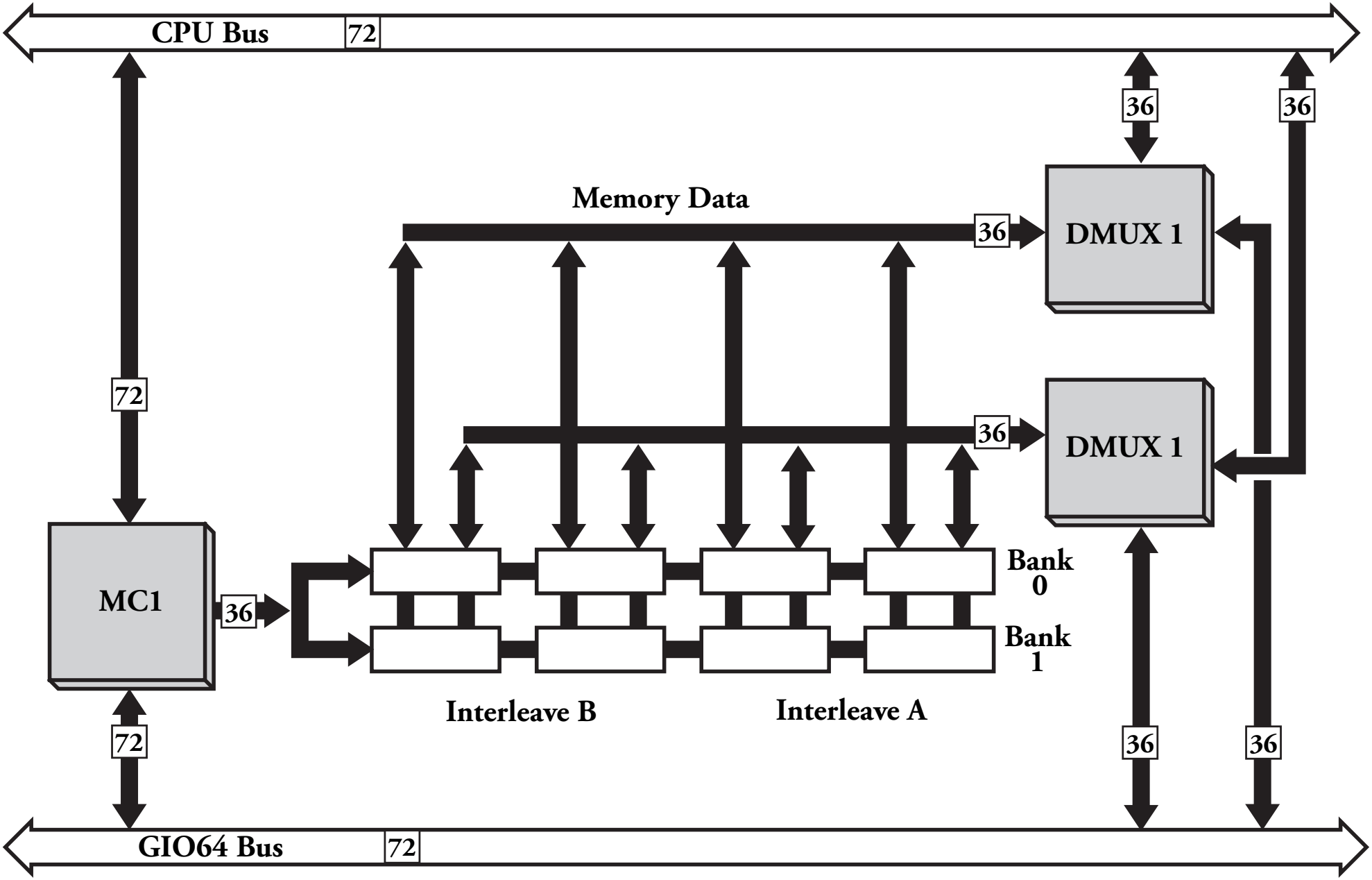
CPU Bus
72
36
36
Memory Data
36
DMUX 1
72
36
DMUX 1
MC1
36
Bank
0
Bank
1
Interleave B
Interleave A
72
36
36
GIO64 Bus
72