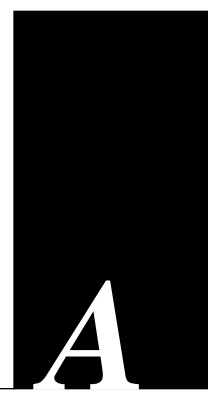# Appendix A
IGS Configuration Registers

Appendix A describes the IGS hardware and software configuration registers, the factory default settings of each, and the procedures for changing those settings.

The hardware configuration register is an 8-bit mechanical switch located on the IGS backpanel. The 16-bit software configuration register resides in nonvolatile memory. The hardware configuration register setting has priority, and will override software configuration register settings if a conflict arises. To avoid such conflicts, only the software register settings that cannot be set by the hardware register are described in this appendix.

Use the processor configuration register information contained in Appendix A to do the following:

■ Set a boot file name

■ Define the Break key

■ Control broadcast addresses

■ Set the console baud rate

■ Enable/disable a watchdog timer

■ Determine the server response to a bootload failure

■ Control factory diagnostic modes in the server

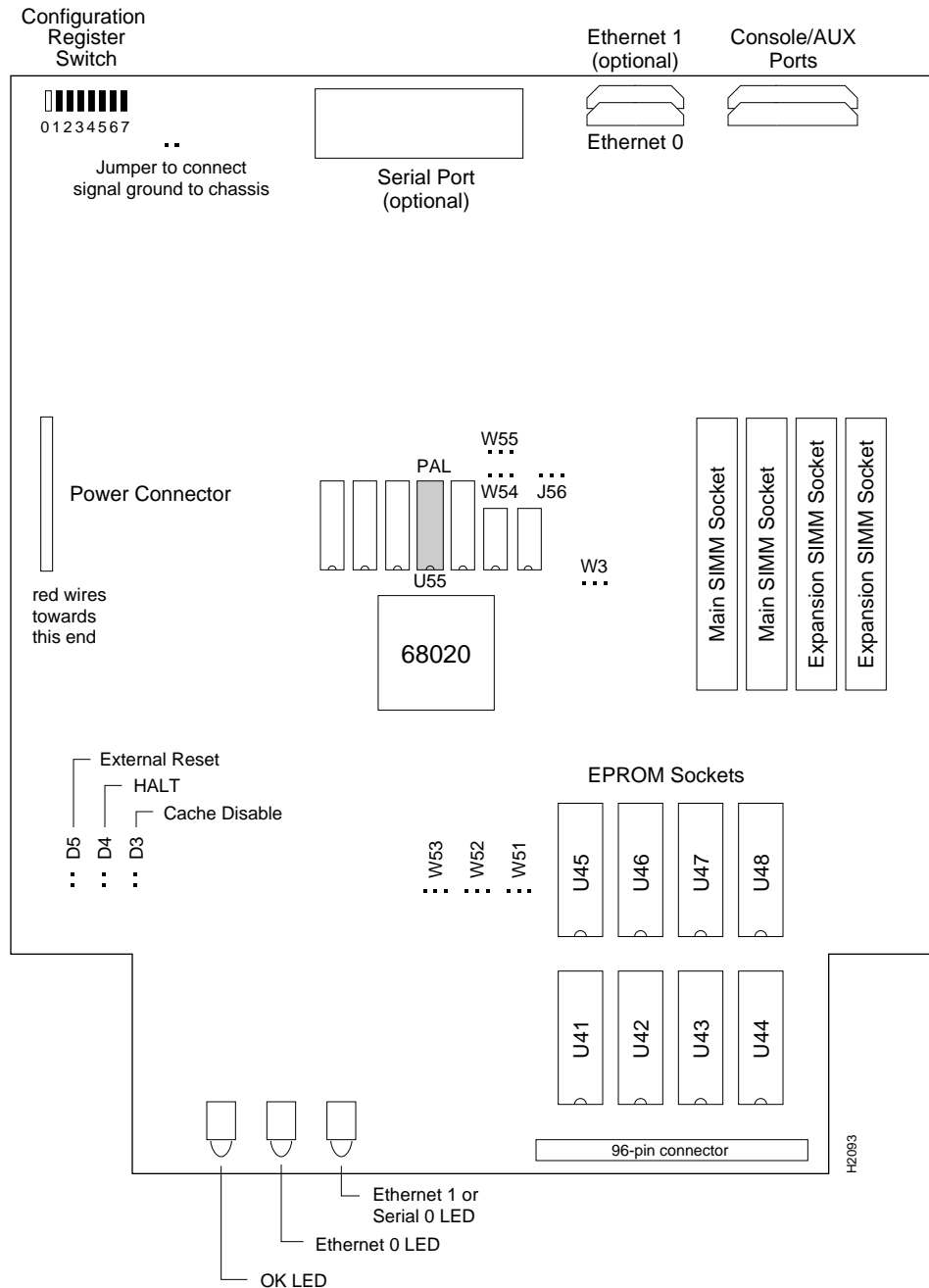Figure A-1 shows the top side of the IGS processor card as viewed with the chassis front facing you.

Configuration Register Switch

01234567

Jumper to connect signal ground to chassis

Serial Port (optional)

Ethernet 1 (optional)

Console/AUX Ports

Ethernet 0

Power Connector

red wires towards this end

W55

PAL

W54   J56

W3

U55

68020

Main SIMM Socket

Main SIMM Socket

Expansion SIMM Socket

Expansion SIMM Socket

External Reset

HALT

Cache Disable

D5 D4 D3

EPROM Sockets

W53 W52 W51

U45   U46   U47   U48

U41   U42   U43   U44

96-pin connector

H2093

Ethernet 1 or Serial 0 LED

Ethernet 0 LED

OK LED

Figure A-1   IGS Card Layout

Hardware Configuration Register

In the back of the chassis under the power switch is an 8-bit switch, the hardware configuration register. The least significant bit of the configuration register is the one labeled "0" in Figure A-2.

Table A-1   Hardware Configuration Bit Meaning

Bit Number	Meaning
00-03	Power-up default action *
04-05	Console line speed
06	Watchdog timer disabled
07	Run diagnostic tests and ignore NVM contents

* May be overridden by the **boot system** command.

Figure A-2 shows the hardware configuration register factory settings.

To set a bit to 1 (on), push the switch down. To clear a bit to 0 (off), push the switch up.

0

7	6	5	4	3	2	1	0
↑	↑	↑	↑	↑	↑	↑	↓ H1641

1

Figure A-2   IGS Hardware Configuration Register Factory Settings

To change configuration register settings, turn off the server, set or clear the bits, and restart the server. Configuration register changes only take effect when the server restarts; that is, when you switch the power off and on or when you issue a reload command from the console.

The lowest four bits of the hardware configuration register (bits 3, 2, 1, and 0) form the *boot field*. The boot field specifies a number in binary. If you set the boot field value to 0, you must boot the operating system manually by giving a **b** command to the system bootstrap program. If you set the boot field value to 1 (the factory default), the server boots using the default ROM software. If you set the boot field to any other bit pattern, the server uses the resulting number to form a boot file name for netbooting.

Note: Cisco recommends a minimum of four megabytes of primary memory if the IGS will be netbooted.

The server creates a boot file name as part of the automatic configuration processes. To form the boot file name, the server starts with Cisco, and links the octal equivalent of the boot field number, a dash and the processor type name. Table A-2 lists the default boot file names or actions for the IGS processor.

Table A-2   Default Boot File Names

Action/File Name	Bit 3	Bit 2	Bit 1	Bit 0
bootstrap mode	0	0	0	0
ROM software*	0	0	0	1
cisco2-igs	0	0	1	0
cisco3-igs	0	0	1	1
cisco4-igs	0	1	0	0
cisco5-igs	0	1	0	1
cisco6-igs	0	1	1	0
cisco7-igs	0	1	1	1
cisco10-igs	1	0	0	0
cisco11-igs	1	0	0	1
cisco12-igs	1	0	1	0
cisco13-igs	1	0	1	1
cisco14-igs	1	1	0	0
cisco15-igs	1	1	0	1
cisco16-igs	1	1	1	0
cisco17-igs	1	1	1	1

* This is the default boot configuration.

Bit 4 and bit 5 in the hardware configuration register determine the baud rate of the console terminal. Table A-3 shows the bit settings for the four available baud rates. The factory default is 9600 baud.

Table A-3   System Console Terminal Baud Rate Settings

Baud	Bit 5	Bit 4
9600	0	0
4800	0	1
2400	1	1
1200	1	0

Bit/ 6 disables the hardware watch-dog timer. This is in the event of a hardware problem causing the watchdog timer to be dysfunctional, which can prevent the unit from initializing. By factory default, bit 6 is cleared to 0.

Bit 7 enables the factory diagnostic mode in the server. Setting this bit causes the server to produce detailed CPU self-check messages, automatically prompt for interface addresses, **not** read configuration files or non-volatile memory, and automatically enable all diagnostic tracing modes. Clearing this bit (the factory default) causes the server to operate normally. Note that setting this switch and reloading your IGS is one way to rewrite your configuration information without using your *privileged* password.

Software Configuration Register

The IGS has a 16-bit software register which is written into the non-volatile memory.

Note: In case of conflict with the hardware configuration register upon reinitialization, the hardware configuration register setting has priority.

Table A-4 indicates the meaning of each of the bits.

Table A-4   Software Configuration Bit Meaning

Bit Number	Meaning
00	Boot from ROM*
01-03	Name of file for Netbooting*
06	Watchdog timer disabled*
07	OEM bit enabled
08	Break Disabled
10	IP broadcast with all zeros
11-12	Console line speed*
13	Boot default ROM software if network boot fails
14	IP broadcasts do not have net numbers
15	Run diagnostic tests and ignore NVM contents*

* These bits are controlled by the hardware configuration register.

To change configuration register settings, use the **config-register** command documented below, and restart the server. Configuration register changes only take effect when the server restarts, that is, when you switch the power off and on or when you issue a **reload** command from the console.

In order to issue the **configure** or **reload** commands, you must first enable the *privileged* mode of operation. At the "GS>" prompt, type "enable." The system will prompt you for the privileged password. After the password has been correctly entered, the prompt will change to a pound sign (#). When you wish to exit the privileged mode, type "disable" at the prompt.

Use the **config-register** *value* configuration command to set the contents of the software configuration register. *Value* is a hexadecimal number preceded by "0x." The software configuration register is stored in nonvolatile memory, as there are no hardware jumpers available. For example, the default switch register contents can be set with the command "config-register 0x1." The new setting does not take effect until the IGS software is reloaded. The **show hardware** command will display the configuration register value stored for the next reload, as well as the value currently in effect.

Bit 8 controls the console Break key. Setting bit 8 (the factory default) causes the processor to ignore the console Break key. Clearing bit 8 causes the processor to interpret Break as a command to force the system into the bootstrap monitor, halting normal operation.

Bit 10 controls the host portion of the Internet broadcast address. Setting bit 10 causes the processor to use all zeros; clearing bit 10 (the factory default) causes the processor to use all ones. Bit 10 interacts with bit 14, which controls the network and subnet portions of the broadcast address. Table A-5 shows the combined effect of bits 10 and 14.

Table A-5   Configuration Register Settings for Broadcast Address Destination

Bit 14	Bit 10	Address (<net> <host>)
off	off	<ones> <ones>
off	on	<zeros> <zeros>
on	on	<net> <zeros>
on	off	<net> <ones>

Bit 13 determines the server response to a bootload failure. Setting bit 13 causes the server to load operating software from ROM after five unsuccessful attempts to load a boot file from the network. Clearing bit 13 causes the server to continue attempting to load a boot file from the network indefinitely. By factory default, bit 13 is cleared to 0.

Initialization and Self Test

The following tests are performed automatically each time the IGS is turned on or reinitialized.

Step 1:   Reset the network A and B interfaces.

Step 2:   Update the 16-bit software configuration register from the 8-bit hardware configuration register.

Step 3:   Initialize the Universal Asynchronous Receiver Transmitter (UARTs).

Step 4:   Print the sign-on message; for example:

```
System Bootstrap, Version 4.2(06)
```

Step 5:   Exit boot state. While in boot state, reads to low memory get mapped to reads in ROM address space.

Step 6:   Set and verify the bus error vector (this is the first time main memory is accessed).

Step 7:   Fill low RAM from 0x10 to 0x1000 with 0x00000000.

Step 8:   Verify that low RAM from 0x10 to 0x1000 is 0x00000000. Fill low RAM from 0x10 to 0x1000 with 0xFFFFFFFF.

Step 9:   Verify that low RAM from 0x10 to 0x1000 is 0xFFFFFFFF.

Step 10:   Fill low RAM from 0x10 to 0x1000 with address+1.

Step 11:   Verify that low RAM has address+1 (assures unique addressability).

Step 12:   Size memory by detecting bus errors and wraparound.

Step 13:   Initialize the rest of RAM space.

Step 14:   Copy MC68020 CPU exception vectors from ROM to RAM.

Step 15: Start the realtime clock.

Step 16: Perform the go/nogo test of realtime clock by ensuring that clock increments.

Step 17: Start watchdog timer (The card resets if the watchdog expires).

Step 18: Determine NVRAM size (there are versions of the IGS with 16 KB and 32 KB NVRAM).

Step 19: Search for a system image in ROM address space.

Step 20: Initialize ROM monitor variables.

Step 21: Read to identify our configuration for system software (1E1T or 2E).

Step 22: Save boots/reboot information for **show hardware** and **show stacks**.

Step 23: Light the OK LED.

Step 24: Return to the monitor routine which will boot a system image or start up the ROM monitor command interpreter.

If you set the DIAG bit in the hardware configuration register, the console terminal displays:

```
System Bootstrap, Version 4.2(563), INTERIM SOFTWARE
Exiting boot state - setting bus error vector..[OK]
Testing low memory...0's...1's...address+1...[OK]
Sizing memory...writing...reading...at 0x100700, expected 0x400,
got 0xFFFF602E 1024 pages...[OK]
Setting memory to all ones...[OK]
Setting up exception vectors...[OK]
Enabling timers...[OK]
Enabling Watchdog timer...[OK]
Sizing NVRAM...found 16K bytes of NVRAM[OK]
Searching for system code...[OK]
Setting up monitor variables...[OK]
Reading Identity register...Rev I or Rev II [OK]
Exiting to monitor command level
IGS processor with 1024 Kbytes of memory
>
```

Note: The same tests are performed if the DIAG bit is not set, but the results are not displayed on the screen.