CHAPTER 1

Product Overview

The Cisco 7507 router provides high reliability, availability, serviceability, and performance. The system supports multiprotocol, multimedia routing, and bridging with a wide variety of protocols and any combination of Ethernet, Fast Ethernet, Token Ring, Fiber Distributed Data Interface (FDDI), serial, multichannel, channel attachment, and High-Speed Serial Interface (HSSI) media. Network interfaces reside on modular interface processors, which provide a direct connection between the two high-speed Cisco Extended Buses (CyBuses) and the external networks.

Online insertion and removal (OIR) allows you to add, replace, or remove interface processors without interrupting the system power or entering any console commands. The redundant power option provides dual load-sharing power supplies that maintain input power without interruption if one supply fails. Environmental monitoring and reporting functions enable you to maintain normal system operation by resolving adverse environmental conditions prior to loss of operation. If conditions reach critical thresholds, the system shuts down to avoid equipment damage from excessive heat or electrical current.

This chapter provides physical and functional overviews to familiarize you with your new system. It contains physical descriptions of the system hardware and major components, and functional descriptions of hardware-related features. Descriptions and examples of software commands appear only when they are necessary for installing or maintaining the system hardware. For complete command descriptions and instructions, refer to the related software reference publications.

Following is a list of acronyms that identify the system components and features:

- CxBus—Cisco Extended Bus, 533-megabits-per-second (Mbps) data bus for interface processors (used in the Cisco 7000 series)
- CyBus—Cisco Extended Bus, 1.067-gigabits-per-second (Gbps) data bus for interface processors (two CyBuses are used in the Cisco 7507)
- AIP—Asynchronous Transfer Mode (ATM) Interface Processor
- CIP—Channel Interface Processor
- EIP—Ethernet Interface Processor
- FIP—FDDI (Fiber Distributed Data Interface) interface processor
- FEIP—Fast Ethernet Interface Processor
- FRU—Field-replacable unit; intended to be replaced by Cisco-certified service providers only
- FSIP—Fast Serial Interface Processor
- HIP—High-Speed Serial Interface (HSSI) interface processor
- MIP—MultiChannel Interface Processor

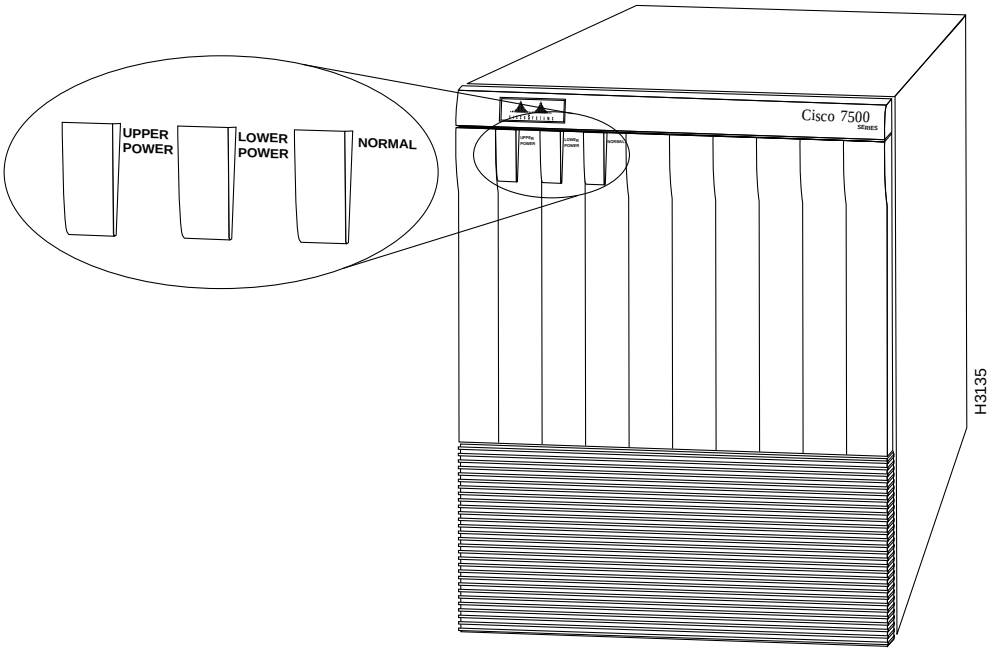
- OIR—Online insertion and removal, the feature that allows you to replace interface processors and redundant power supplies without interrupting system power
- PA—Port adapter, daughter cards used on a number of the interface cards in the chassis
- RSP2—Route Switch Processor, the system processor board
- Spare—A spare part, component, or entire assembly whose replacement does not require a Cisco-certified service provider
- TRIP—Token Ring Interface Processor

Physical Description

The router front panel, shown in Figure 1-1, contains three status indicators and two removable panels for access to the internal components. The three light emitting diodes (LEDs) on the front panel indicate normal system operation and the currently active power supplies. On the back of the router, additional LEDs on the RSP2 and power supplies indicate the same status.

The normal LED goes on to indicate that the system is in a normal operating state and is receiving +5-volts direct current (VDC) from the power supplies. The upper power and lower power LEDs go on to indicate that a power supply is installed in the indicated power supply bay and is providing power to the system. The power LEDs go out if the power supply in the corresponding bay reaches an out-of-tolerance temperature or voltage condition. (For descriptions of thresholds and status levels, refer to the section “Environmental Monitoring and Reporting Functions” in this chapter.) The front-panel normal LED is controlled by the RSP2, which contains an identical normal LED that can be seen from the rear of the router.

Figure 1-1 Router Front View



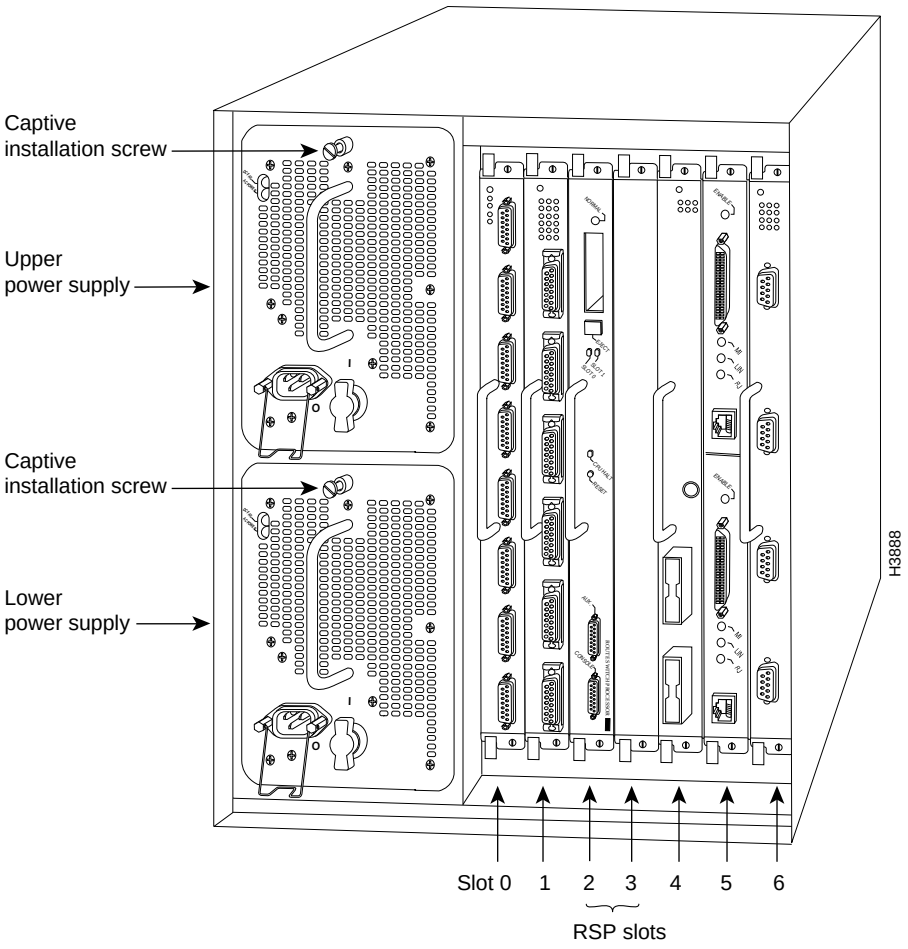
The rear, or interface processor end, of the router, shown in Figure 1-2, provides access to the seven processor slots and removable power supplies. The lower power supply bay contains the first (standard equipment) power supply, and the upper bay contains the second power supply (optional equipment in systems with redundant power). The processor slots contain up to two RSP2s and up to five network interface processors (collectively referred to as *processor modules*).

When viewing the router from the rear, a single RSP2 is always located in slot 2 or 3.

Note Capability to support a second, redundant RSP2 will be added in a later Cisco Internetwork Operating System (Cisco IOS) release.

The remaining five slots are numbered 0 and 1, and 4 through 6, from left to right, viewing the chassis as shown in Figure 1-2. These interface processor slots support any combination of supported network interface types. The RSP2 and interface processors are keyed with guides on the backplane to prevent them from being fully inserted in the wrong slot. RSP2s can only be inserted in slots 2 and 3 and interface processors can only be inserted in slots 0 and 1 and slots 4 through 6. The RSP2 and interface processors are described in the sections that follow.

Figure 1-2 Router Rear View



The RSP2 and interface processors slide into slots in the rear of the router and connect directly to the CyBus backplane; there are no internal cables to connect. Spring-loaded ejector levers help to ensure that a processor module is either fully connected to the backplane or fully disconnected from it. Captive installation screws at the top and bottom of each processor module faceplate also ensure proper seating in the backplane, and prevent the processor module from disengaging from the backplane. (The system might hang if a processor module pulls away from the backplane and intermittently breaks the connection between the processor module connector and the backplane pins.) Empty slots contain a blank board carrier to maintain proper airflow through the chassis. These blanks are interface processor and RSP2 carriers without boards, LEDs, or connectors.

Chassis Specifications

The system physical specifications and power requirements are listed in Table 1-1.

Table 1-1 Router Physical Specifications

Description	Specifications
High-speed backplane	1.067-Gbps CyBus (the 7507 has dual CyBuses), 7 slots
Dimensions (H x W x D)	19.25 x 17.5 x 25.1" (48.90 x 44.45 x 63.75 cm) Chassis depth including power cable is 28" (71.12 cm).
Weight	Chassis only: 76 lb (34.47 kg) Chassis fully configured with 2 RSP2 and 5 interface processors, and 2 power supplies: 145 lb (65.76 kg)
DC-input voltage	–40 volts direct current (VDC) minimum –48 VDC nominal –72 VDC maximum
DC voltages supplied and steady-state maximum current ratings	+5.2V @ 100 amps (A) +12V @ 15A –12V @ 3A +24V @ 5A
DC-input power	1000 watts (W)
DC-input power supply hold-up time specification	10 milliseconds (ms) of output after the input has been interrupted
DC-input wiring	8 AWG (American Wire Gauge) wire that you provide
Power supply	700W maximum (AC-input and DC-input power supplies)
Power dissipation	626W maximum configuration, 530W typical with maximum configuration
Heat dissipation	1200W (4100 Btu/hr)
Input voltage	100 to 240 VAC wide input with power factor correction (PFC)
Frequency	50 to 60 Hz (hertz) autoranging
AC current rating	12A maximum at 100 VAC, 6A maximum at 240 VAC with the chassis fully configured
Airflow	140 cfm (cubic feet per minute) through the system blower
Operating temperature	32 to 104 F (0 to 40 C)
Nonoperating temperature	–4 to 149 F (–20 to 65 C)
Humidity	10 to 90%, noncondensing
Agency approvals	Safety: UL 1950, CSA 22.2-950, EN60950: 1992 EMI: FCC Class A, EN55022 Class B, VCCI Class 2

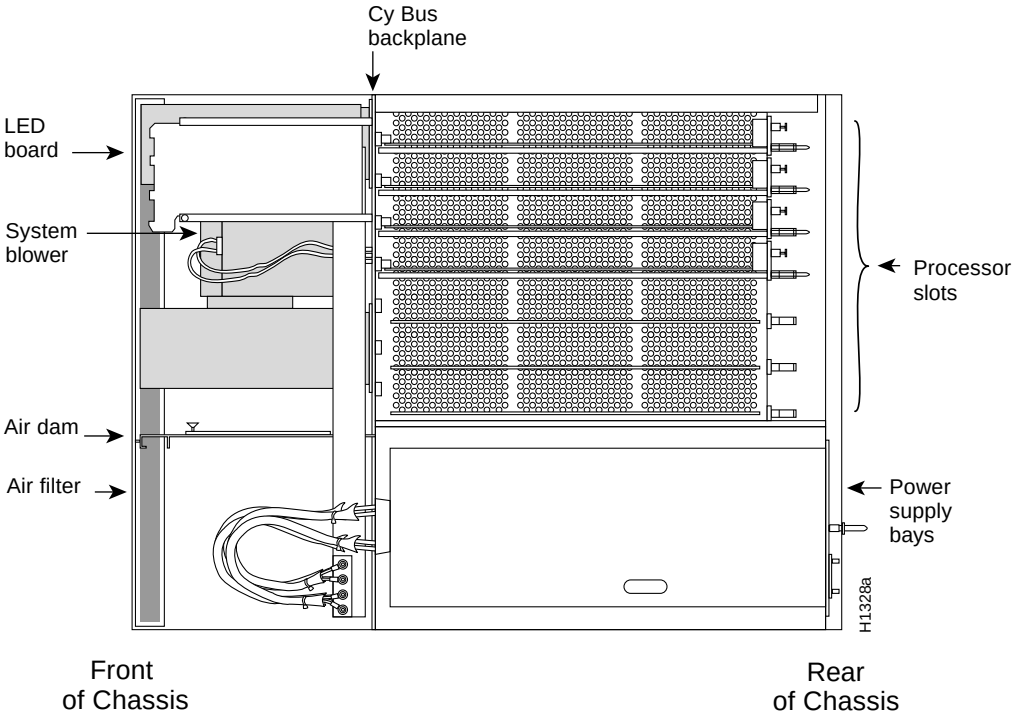
The router operates as either a freestanding or rack-mounted unit. An optional rack-mount kit is available for mounting the chassis in an EIA-310C standard 19-inch equipment rack. When the system is not mounted in a rack, place it on the floor or on a sturdy platform.

The top-down view of the chassis shown in Figure 1-3 illustrates the locations of the main system components. The dual arbiter board (which provides CyBus arbitration), the chassis interface board (which contains the environmental monitoring functions), the LED board, and the system blower are located inside the left front of the chassis behind removable front panels.

The blower moves cooling air through the chassis and across the processor modules to prevent components on the boards from overheating. The power supply bays are located next to interface processor slot 0 and are accessible from the rear of the chassis. An air dam keeps cooling air drawn in by the system blower separate from that drawn in by the power supply fans. (Refer to the section "Power Supplies" in this chapter.)

One 700-watt (W), AC-input or DC-input power supply is standard equipment in the router. A second, *identical* power supply provides a redundant power option. Load sharing and redundancy are automatically enabled when a second power supply is installed; no configuration is required. Each supply has an individual power switch and status LEDs. When only one power supply is used, it should be installed in the bottom power supply bay to maintain a low center of gravity in the router chassis.

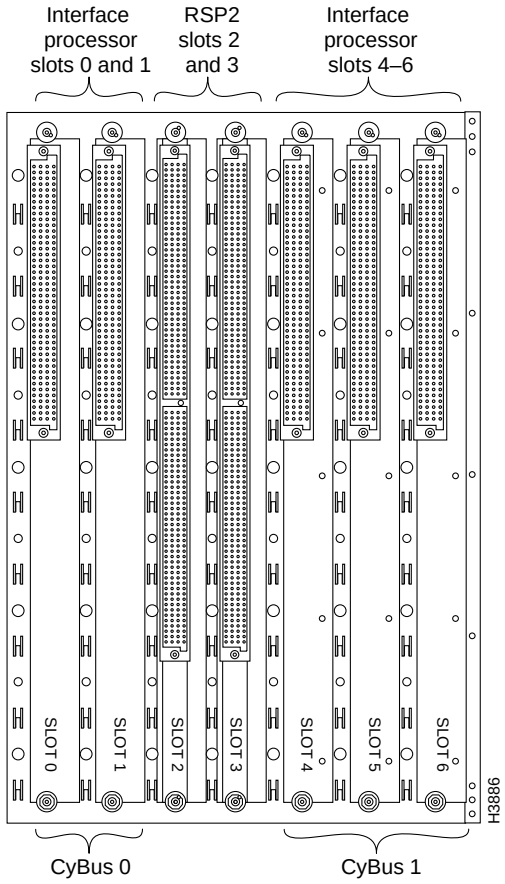
Figure 1-3 Router Top-Down View



System Backplane

The dual-CyBus backplane in the Cisco 7507 has an aggregate bandwidth of 2.134 Gbps. Interface processor slots 0 and 1 comprise CyBus 0, and interface processor slots 4 through 6 comprise CyBus 1. Figure 1-4 shows the orientation of the two CyBuses.

Figure 1-4 CyBus 0 and CyBus 1 Orientation on the Backplane



The RSP2 provides distributed processing and control for the interface processors, and controls communication between high-speed interface processors (interface processor-to-interface processor) and the system processor (interface processor-to-system processor).

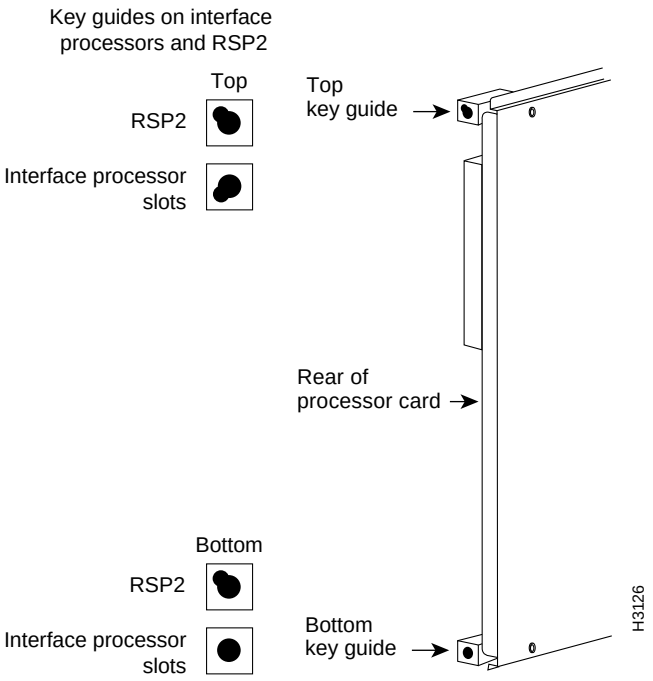
Note An RSP2 in either slot 2 or slot 3 controls both CyBus 0 and CyBus 1.

Interface processors connected to one CyBus are unaffected by the traffic generated by the interface processors connected to the other CyBus. The two CyBuses are independent of one another.

A chassis identification (memory) device on the backplane contains a bank of hardware (MAC-layer) addresses for the interface processor ports, as well as chassis-specific information.

The backplane slots are keyed so that the processor modules can be installed only in the slots designated for them. Keys on the backplane fit into two key guides on each module. (See Figure 1-5.) These key guides apply to the corresponding blank carriers: MAS-RSPBLANK= for the RSP2 slots and MAS-7KBLANK= for the interface processor slots.

Figure 1-5 Backplane Slot Keys



Caution When installing an RSP2 or interface processor, ensure that you are installing it in the appropriate slot to avoid damaging the key guides or the backplane. Be sure to install an RSP filler (MAS-RSPBLANK=) in the empty RSP slot. Interface processor fillers (MAS-7KBLANK=) will not fit in the RSP slots.

Dual Arbiter

The dual arbiter, which arbitrates traffic on the dual CyBuses and generates the CyBus clocks, is a printed circuit board that resides on the front of the system backplane inside the front chassis compartment. (See Figure 1-3.) The dual arbiter is a not a spare part; it is a FRU. The dual arbiter arbitrates traffic across the CyBuses by prioritizing access requests from interface processors to ensure that each request is processed and to prevent any interface processor from jeopardizing the CyBus and interfering with the ability of the other interface processors to access the RSP2. Following is a summary of the services that the dual arbiter provides:

- CyBus clock generation—Generates the clock and provides a private copy of the clock to the RSP2 and each interface processor.
- CyBus arbitration—Arbitrates interface processor requests to transmit commands on the CyBus. The arbitration is based on a round-robin priority scheme to ensure that all interface processors have access to a known portion of the CyBus bandwidth.
- Global lock arbitration—Arbitrates interface processor requests for the global lock, a synchronization primitive used to control interface processor access to shared data structures.

Chassis Interface

The chassis interface provides the environmental monitoring (ENVM) and power supply monitoring functions for the Cisco 7507. (See Figure 1-3 for its relative location.) The chassis interface is not a spare part; it is a FRU.The chassis interface isolates the CPU and system software from chassis-specific variations. The chassis interface attaches directly to the system backplane.

The functions of the chassis interface are as follows:

- Report backplane type.
- Report dual arbiter type.
- Monitor power supply status.
- Monitor fan/blower status.
- Monitor temperature sensors on the RSP2.
- Provide router power up/down control.
- Provide power supply power-down control.

Power Supplies

The router comes equipped with one 700W, AC-input or DC-input power supply. An optional second identical power supply also is available for redundant power. Dual power supplies are automatically load sharing and redundant, which means a second power supply can be installed or replaced without interrupting system operation. Power supplies are available as spare parts.

Caution To prevent problems, do *not* mix DC-input and AC-input power supplies in the same chassis. Your Cisco 7507 must have *either* DC-input or AC-input power supplies.

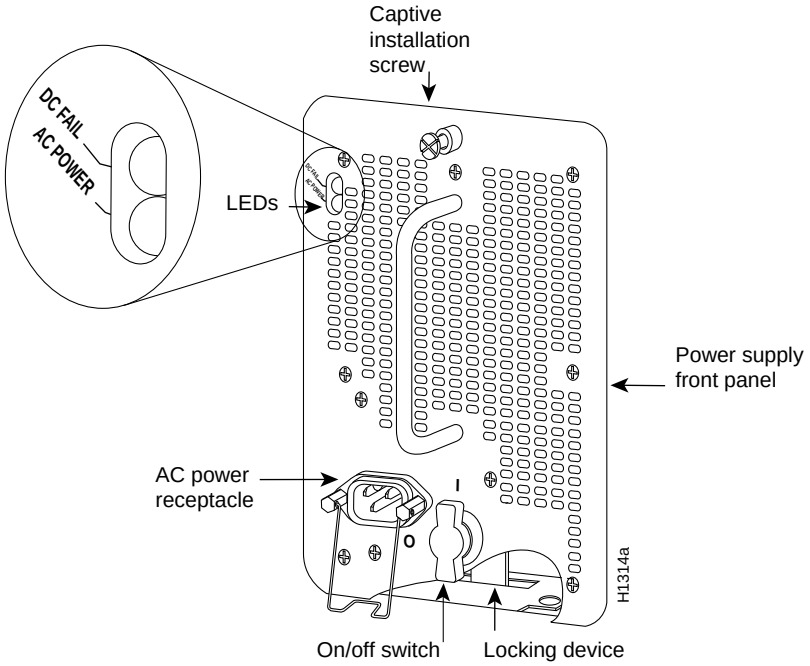
Each power supply should be connected to a separate power source so that, in case of an input power line or power supply failure, the second power supply maintains uninterrupted system power.

Caution When only one power supply is used, install it in the lower power supply bay to maintain a low center of gravity in the chassis.

You must turn the power (on/off) switch (shown in Figure 1-6) to the off (O) position before you can remove the power supply from the chassis. When the power supply switch is in the on (|) position, a locking device on the switch slides into a slot in the power supply bay to lock the power supply in the chassis. (See Figure 1-6.) When the switch is in the off (O) position, the tab retracts so that you can slide the power supply out.

Caution Always tighten the captive installation screw at the top of the power supply; it ensures that the supply is securely seated in the bay and provides proper grounding. (See Figure 1-6.)

Figure 1-6 Power Supply Faceplate (AC-Input Power Supply Shown)



On the router front panel, the upper power and lower power LEDs go on when the power supply in the corresponding bay is installed and supplying power to the system. Both the upper and lower power LEDs should go on in systems with redundant power. All power-related LEDs are described in the appendix “Reading LED Indicators.”

The power supplies are self-monitoring. Each supply monitors its own temperature and internal voltages. For a description of power supply shutdown conditions and thresholds, refer to the section “Environmental Monitoring and Reporting Functions” in this chapter.

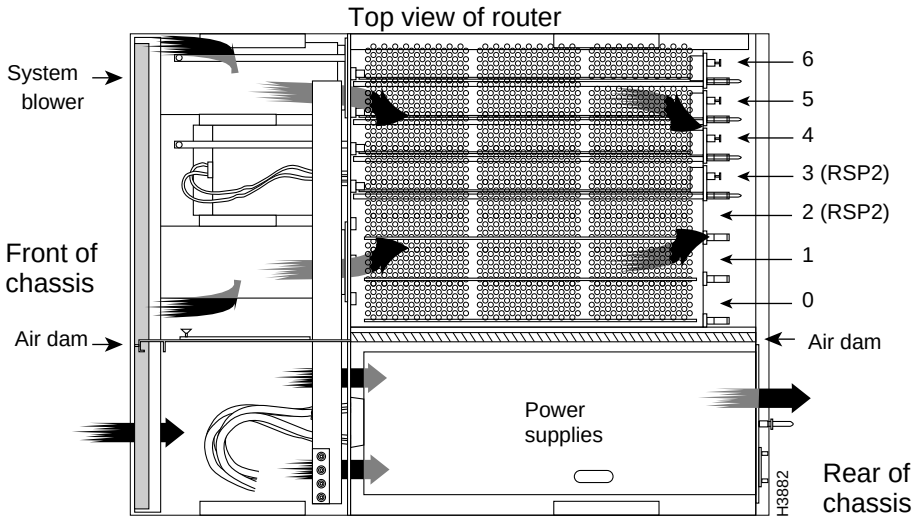
For AC-input power supplies, a modular power cable connects each power supply to the site power source. A cable retention clip on the power supply AC receptacle prevents the cable from accidentally being pulled out.

For DC-input power supplies, you supply the power cable based on the specifications provided in Table 1-1. Strain relief is provided by two nylon cable ties that you provide. For power supply installation procedures refer to the section “Installing Power Supplies” in the chapter “Installing the Router.”

System Blower

The system blower provides cooling air for the processor modules. The blower is located inside the front chassis compartment as shown in Figure 1-7. An internal fan in each power supply draws cooling air from the front of the chassis, through the power supply, and out the back of the chassis. An air dam keeps the power supply airflow separate from that of the rest of the chassis, which is cooled by the system blower. (See Figure 1-7.)

Figure 1-7 Internal Airflow (Top-Down View)



The blower draws air in through the air filter in the front chassis panel and directs it up through the floor of the internal slot compartment and over the boards. The exhaust air is forced out the rear of the chassis above and to each side of the processor slots. Figure 1-7 shows the airflow path.

The blower needs a clean air filter in order to draw in sufficient amounts of cooling air; excessive dust in the filter will restrict the airflow. Keep the air filter clean and replace it when needed. the chapter “Maintaining the Router” provides air filter cleaning and replacement procedures. The blower is available as a spare part.

Sensors on the RSP2 monitor the inlet and internal chassis air temperatures. If the air temperature at either of the sensors exceeds a desired threshold, the environmental monitoring system displays warning messages and can interrupt system operation to protect the system components from possible damage from excessive heat or electrical current. For specific threshold and status level descriptions, refer to the section “Environmental Monitoring and Reporting Functions” in this chapter.

Route Switch Processor (RSP)

The RSP2 shown in Figure 1-8 is the main system processor in the router. The RSP2 contains the system CPU and system memory components. It maintains and executes the management functions that control the system. The system software is contained on the RSP2 in either a Flash memory, single in-line memory module (SIMM) or in a Personal Computer Memory Card International Association (PCMCIA) Flash memory card.

The RSP2 contains the following components:

- Orion/R4600 Reduced Instruction Set Computing (RISC) processor, used for the central processing unit (CPU). The CPU runs at an external clock speed of 50 megahertz (MHz) and an internal clock speed of 100MHz.
- Most of the memory components used by the system, including the onboard Flash memory SIMM.
- Air-temperature sensors for environmental monitoring.

In addition to the preceding system components, the RSP2 contains and executes the following management functions that control the system:

- Sending and receiving routing protocol updates
- Managing tables and caches
- Monitoring interface and environmental status
- Providing Simple Network Management Protocol (SNMP) management and the console/Telnet interface

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Note The RSP2 *must* be installed in RSP slot 2 or RSP slot3. (Refer to Figure 1-4.) During operation, the system will hang if the connection between the RSP2 connector and any of the backplane pins is interrupted. To maintain proper airflow through the chassis and card cage in systems with a single RSP2, an RSP filler blank (MAS-RSPBLANK=) is required in the RSP slot adjacent to the RSP2. A blank ships with each single-RSP2 system.

The high-speed switching section of the RSP2 communicates with and controls the interface processors on the CyBus. This section decides the destination of a packet and switches the packet based on that decision. The RSP2 uses a 16-million-instructions-per-second (mips) processor to provide high-speed, optimum switching and routing. The single enabled LED goes on to indicate that the RSP2 is receiving +5V and enabled for operation.

Memory Components

Figure 1-8 shows the locations of the various types of memory on the RSP2, and Table 1-2 lists the functions of each.

Figure 1-8 Route Switch Processor (Horizontal Orientation)

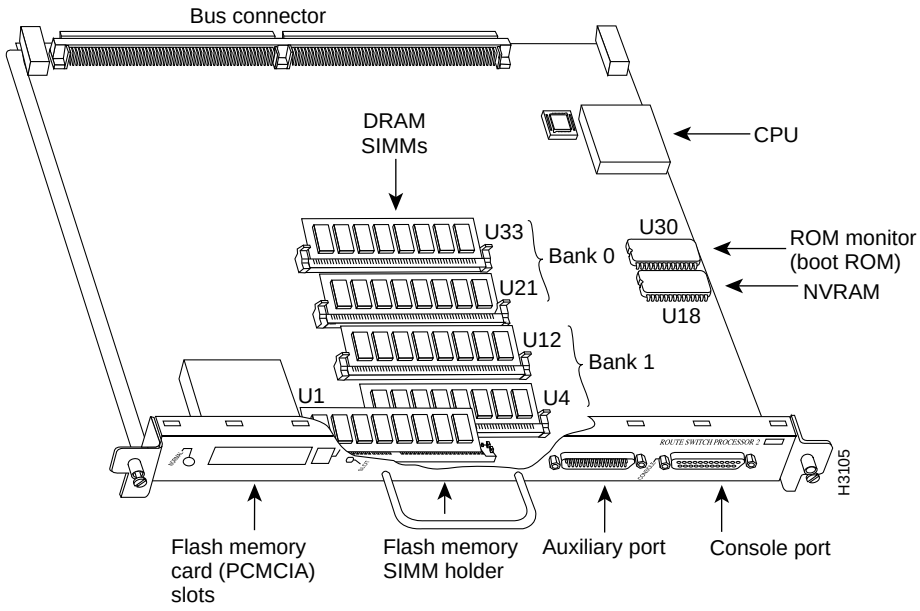


Table 1-2 RSP2 Memory Components

Type	Size	Quantity	Description	Location
DRAM[1]	16 to 128 MB[2]	2 to 4	8, 16, or 32-MB SIMMs (based on maximum DRAM required).	Bank 0: U21 and U33 Bank 1: U4 and U12
NVRAM[3]	128 KB[4]	1	Nonvolatile EPROM[5] for the system configuration file.[6]	U18
Flash SIMM Flash Card	8 MB 8, 16, and 20 MB[7]	1 Up to 2	Contains the Cisco IOS images on the RSP2. Contains the Cisco IOS images on up to two PCMCIA cards.	U1 Slot 0 and Slot 1
Boot ROM[8]	256 KB	1	EPROM for the ROM monitor program.	U30

1. Dynamic random-access memory.
2. MB = megabyte.
3. NVRAM = nonvolatile read-only memory.
4. KB = kilobyte.
5. EPROM = erasable programmable read-only memory.
6. A system configuration file is contained in NVRAM, which allows the software to control several system variables.
7. Only Intel Series 2+ Flash memory cards can be used with the RSP2.
8. ROM = read-only memory.

System Software

The Cisco 7507 router supports downloadable system software and microcode for most upgrades; you can remotely download, store, and boot from a new image. Upgrade documentation accompanies all upgrade kits, and provides instructions for upgrading software from either floppy disks or over the network.

Flash memory on the RSP2 contains the default system software. An EPROM device on each interface processor contains the latest interface processor microcode version in compressed form. At system startup, an internal system utility scans for compatibility problems between the installed interface processor types and the bundled microcode images, then decompresses the images into running memory (DRAM). The bundled microcode images then function the same as images loaded from the microcode EPROM.

DRAM

DRAM stores routing tables, protocols, and network accounting applications. The standard RSP2 configuration is 16 MB of DRAM, with up to 128 MB available through SIMM upgrades.

Note When upgrading DRAM, you must use SIMMs from an approved vendor. To ensure that you obtain the most current vendor information, obtain the list from Customer Information Online (CIO) or the Technical Assistance Center (TAC). To contact CIO or the TAC, refer to the "Service and Support" card in the Warranty Pack that accompanied your new Cisco 7507 system.

NVRAM

The NVRAM stores the system configuration and the environmental monitoring logs, and is backed up with built-in lithium batteries that retain the contents for a minimum of five years. When replacing an RSP2 in a Cisco 7507 with a single RSP2, be sure to back up your configuration to a remote server so that you can retrieve it later. (See the Timesaver note that follows.)

Timesaver Before replacing an RSP2 in a system with a single RSP2, back up the running configuration to a Trivial File Transfer Protocol (TFTP) file server or flash card so that you can later retrieve it. If the configuration is not saved, the entire configuration will be lost—inside the NVRAM on the removed RSP2—and you will have to reenter it manually. This procedure is not necessary if you are temporarily removing an RSP2; lithium batteries retain the configuration in memory until you replace the RSP2 in the system.

Flash Memory

Either the imbedded (onboard) Flash memory (on a SIMM) or the Flash memory on a Flash memory (PCMCIA) card, allows you to remotely load and store multiple Cisco IOS software and microcode images. You can download a new image over the network or from a local server and then add the new image to Flash or replace the existing files. You can then boot routers either manually or automatically from any of the stored images. Flash memory also functions as a TFTP server to allow other servers to remotely boot from stored images or to copy them into their own Flash memory.

EEPROM

An electrically erasable programmable read-only memory (EEPROM) component on the RSP2 (and each interface processor) stores board-specific information such as the board serial number, part number, controller type, hardware revision, and other details unique to each board.

Note This EEPROM is not a spare part or a FRU and cannot be programmed in the field.

Jumpers

Because the RSP2 uses a software configuration register for system configuration and Flash memory for system software images, there are no user-configurable jumpers on the RSP2.

LEDs

The two LEDs on the RSP2 indicate the system and RSP2 status. The normal LED is on when the system is operational; during normal operation the CPU halt LED should be off. The CPU halt LED, which goes on only if the system detects a processor hardware failure, should never be on. For complete descriptions of the LED states, refer to the appendix "Reading LED Indicators."

Serial Ports

Two asynchronous EIA/TIA-232 serial ports on the RSP2, the console and auxiliary ports, provide the means for connecting a terminal, modem, or other device for configuring and managing the system. A data circuit-terminating equipment (DCE) EIA/TIA-232 receptacle console port on the RSP2 provides a direct connection for a console terminal.

Note EIA/TIA-232 was known as recommended standard RS-232 before its acceptance as a standard by the Electronic Industries Association (EIA) and Telecommunications Industry Association (TIA).

The adjacent data terminal equipment (DTE) EIA/TIA-232 plug auxiliary port supports flow control and is often used to connect a modem, a channel service unit (CSU), or other optional equipment for Telnet management of the attached device.

The console and auxiliary ports support asynchronous transmission. Asynchronous transmission uses control bits to indicate the beginning and end of characters rather than precise timing. The serial interface ports on the FSIP support synchronous transmission, which maintains precise clocking between the transmitter and receiver by sending frames of information that comprise separate clock signals along with the data signals. When connecting serial devices, ensure that the devices support the proper transmission timing methods for the respective port: asynchronous for the console and auxiliary ports, and synchronous for the FSIP and MIP serial ports.

Interface Processors

An interface processor consists of a modular, self-contained interface board and one or more network interface connectors in a single 11 x 14-inch unit. All interface processors support OIR, so you can install and remove them without opening the chassis and without turning off the chassis power.

Following are descriptions of the interface processors:

- AIP—Asynchronous Transfer Mode (ATM) Interface Processor. For interface types and specifications, refer to the section "AIP Connection Equipment" in the chapter "Preparing for Installation."
- CIP—Channel Interface Processor. Any combination of one or two bus and tag and/or one or two Enterprise System Connection (ESCON) interfaces. For bus and tag and ESCON interface configurations and specifications, refer to the configuration note *Channel Interface Processor (CIP) Installation and Configuration* (Document Number 78-1342-xx).
- EIP— High-speed (10 Mbps) Ethernet Interface Processor with two, four, or six AUI ports.
- FEIP—For up to two 100BASE-T, RJ-45 or Media Independent Interface (MII) ports, which each operate at 100 megabit-per-seconds (Mbps), half or full duplex.
- FIP—High-speed (100 Mbps) FDDI interface processor with one single attachment or dual attachment port (PHY A/PHY B) in any combination of single-mode and multimode ports (such as single-single, multi-single, and so forth).
- FSIP—Fast (up to 8 Mbps, or 16 Mbps aggregate with 8 ports) Serial Interface Processor that provides four or eight synchronous serial ports, using EIA/TIA-232, EIA/TIA-449, EIA-530, E1-G.703/G.704, V.35, and X.21 interfaces.

Caution The early serial interface processor (SX-SIP or PRE-FSIP) cannot be used in the Cisco 7507. (The SX-SIP requires the SxBus and SxBus connectors that are not present in the Cisco 7507.)

- HIP—High-Speed (up to 52 Mbps) Serial Interface (HSSI) Interface Processor with a single HSSI port.
- MIP—For up to two channelized T1 interfaces that operate at T1 speed—up to 1.544 Mbps, or up to two channelized E1 interfaces that operate at E1 speed—up to 2.048 Mbps

Note T1 and E1 interfaces cannot be mixed on a single MIP.

- TRIP—High-speed (4 or 16 Mbps) Token Ring Interface Processor with two or four DB-9 ports.

Interface Processor Microcode

The microcode on each interface processor contains board-specific software instructions. New features and enhancements to the system or interfaces are often implemented in microcode upgrades.

The Cisco 7507 supports downloadable microcode, which enables you to download new microcode images remotely and store them in Flash memory. You can then use software commands to load a specific microcode image from Flash memory or to load the default microcode image from ROM.

Note We strongly recommend that the microcode bundled with the system software be used as a package. Overriding the bundle could possibly result in incompatibility between the various interface processors in the system.

System software upgrades also can contain upgraded microcode images, which will load automatically when the new software image is loaded. With this downloadable microcode feature, you will probably never need to replace the microcode ROM on the board. If replacement is necessary in the future, refer to the section “Microcode Component Replacement” in the chapter “Maintaining the Router.” Specific instructions will also be provided with the replacement component in an upgrade kit.

Interface Processor LEDs

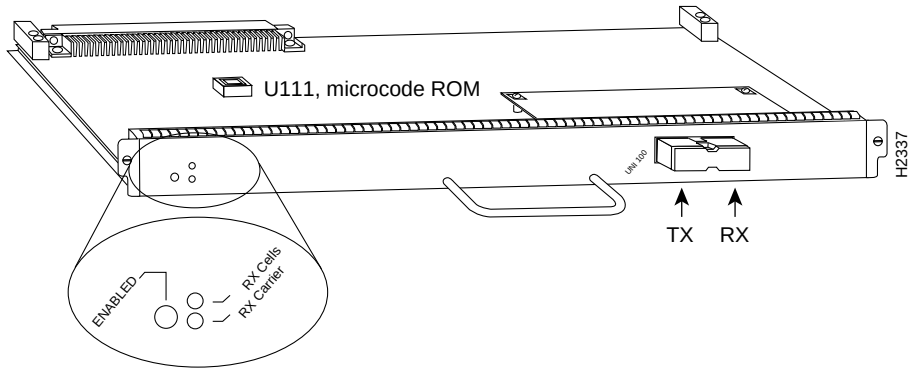
Each interface processor has a unique bank of status LEDs, and all have a common enabled LED at the top of the interface processor face plate. The enabled LED goes on when the RSP2 has completed initialization of the interface processor for operation, indicating that, as a minimum, the interface processor is correctly connected to the backplane, that it is receiving power, and that it contains a valid microcode version. If any of these conditions is not met, or if the initialization fails for other reasons, the enabled LED does not go on. Additional LEDs on each interface processor type indicate the state of the interfaces.

The following sections describe each interface processor type. The appendix “Reading LED Indicators” describes the specific LED states of each.

ATM Interface Processor (AIP)

The AIP provides a direct connection between the high-speed CyBus and the external networks. (See Figure 1-9.) The AIP can support the following data transmission rates: Transparent Asynchronous Transmitter/Receiver Interface (TAXI) 4B/5B at 100 Mbps, Synchronous Optical Network/Synchronous Digital Hierarchy (SONET/SDH) at 155 Mbps, E3 at 34 Mbps, and DS3 at 44.736 Mbps (20 parts per million [ppm]). The default AIP microcode resides on an EPROM in socket U111.

Figure 1-9 ATM Interface Processor (User-to-Network Interface PLIM Shown)



The specific physical layer interface module (PLIM) on the AIP determines the type of ATM connection. There are no restrictions on slot locations or sequence; an AIP can be installed in any available interface processor slot. The AIP supports the following features:

- Multiple rate queues.
- Reassembly of up to 512 buffers simultaneously. Each buffer represents a packet.
- Support for up to 2,048 virtual circuits.
- Support for both ATM adaptation layer (AAL) 5 and AAL3/4.
- Exception queue, which is used for event reporting. Events such as CRC errors are reported to the exception queue.
- Raw queue, which is used for all raw traffic over the ATM network. Raw traffic includes operation and maintenance (OAM) cells and Interim Local Management Interface (ILMI) cells. (ATM signaling cells are not considered raw.)

Following are the product numbers associated with the AIP:

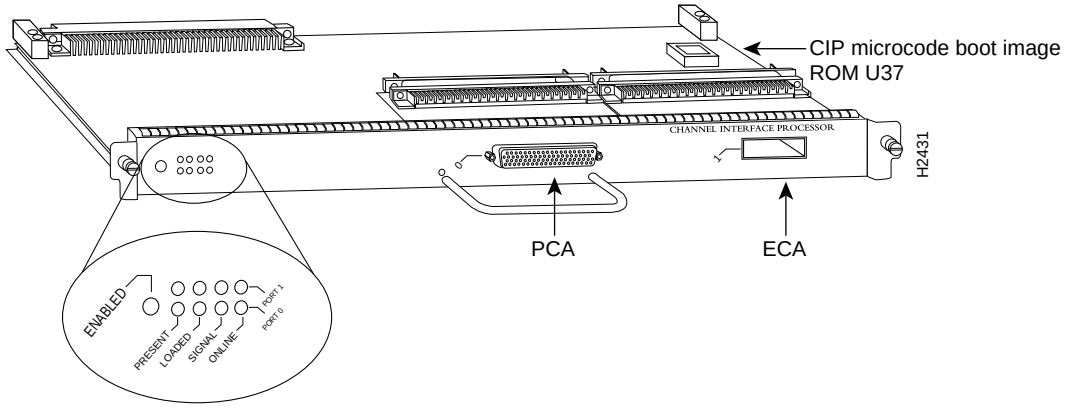
- CX-AIP-TM= (TAXI 4B/5B 100-Mbps multimode fiber-optic cable)
- CX-AIP-SM= (SONET/SDH 155-Mbps multimode fiber-optic cable—STS-3C or STM-1)
- CX-AIP-SS= (SONET/SDH 155-Mbps single-mode fiber-optic cable—STS-3C or STM-1
- CX-AIP-E3= (E3 34 Mbps coaxial cable—CAB-ATM-DS3/E3=) requires CLIP-E3-EMI=
- CX-AIP-DS3= (DS3 45 Mbps coaxial cable—CAB-ATM-DS3/E3=)

For more information on the AIP, refer to the sections “Distance Limitations” and “AIP Connection Equipment” in the chapter “Preparing for Installation.” Also refer to the *Asynchronous Transfer Mode Interface Processor (AIP) Installation and Configuration* publication (Document Number 78-1214-xx), available on UniverCD or in print.

Channel Interface Processor (CIP)

The CIP provides up to two channel-attached interfaces, eliminating the need for a separate front-end processor. (See Figure 1-10.) The CIP interfaces are combinations of a bus and tag (also called an original equipment manufacturer's interface [OEMI] and a parallel I/O interface) adapter and/or an Enterprise Systems Connection (ESCON) adapter. The bus and tag adapter is called the Parallel Channel Adapter (PCA) and the ESCON adapter is called the ESCON Channel Adapter (ECA). The PCA and ECA connect directly to the CIP, and any combination of the two adapters can be used.

Figure 1-10 Channel Interface Processor (Combination PCA and ECA Shown)



Note The ECA and PCA adapters can be upgraded or replaced in the field by a Cisco-certified maintenance provider *only.* There is no microcode for the Channel Interface Processor (CIP) included in the Cisco 7507 software bundle, which, for the initial release of the Cisco 7507, is Cisco Internetwork Operating System (Cisco IOS) Release 10.3(3.2). A CIP will not operate in a Cisco 7507 system with this Cisco IOS release.

The supported processor input/output architectures for the CIP include ESA/390 for ESCON and System/370, 370/Xa, and ESA/390 for bus and tag. The ESCON interface is capable of a data rate up to 17 megabytes per second (MBps), and the bus and tag interface is capable of a data rate up to 4.5 MBps. Only the CIP microcode boot image resides on an EPROM in socket U37. (See Figure 1-10.) The entire CIP microcode image is located in the software/microcode bundle.

There are three carrier types: PCA-ECA carrier, dual ECA carrier, and dual PCA carrier. Following are the product numbers and carrier types associated with the CIP:

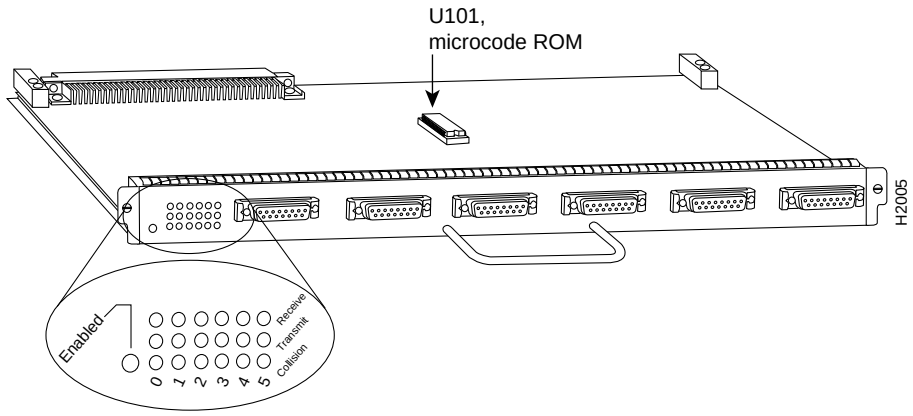
- Single PCA (CX-CIP-PCA1=) on a PCA/ECA carrier
- Combination PCA and ECA (CX-CIP-ECAP1=)
- Single ECA (CX-CIP-ECA1=) on a dual ECA carrier
- Dual ECA (CX-CIP-ECA2=) on a dual ECA carrier
- Dual PCA (CX-CIP-PCA2=) on a dual PCA carrier

For more information on the CIP, refer to the *Channel Interface Processor (CIP) Installation and Configuration* publication (Document Number 78-1342-xx), available on UniverCD, or in print.

Ethernet Interface Processor (EIP)

The EIP, shown in Figure 1-11, provides two, four, or six Ethernet ports that operate at up to 10 Mbps. A bit-slice processor provides a high-speed data path between the EIP and other interface processors. The default EIP microcode resides on an EPROM in socket U101.

Figure 1-11 Ethernet Interface Processor



Each port requires an Ethernet transceiver or a media attachment unit (MAU) and attachment unit interface (AUI) cable to connect to the external network. Following are the product numbers associated with the EIP:

- CX-EIP2= (two Ethernet Version 1 and IEEE 802.3/Ethernet Version 2 interfaces)
- CX-EIP4= (four Ethernet Version 1 and IEEE 802.3/Ethernet Version 2 interfaces)
- CX-EIP6= (six Ethernet Version 1 and IEEE 802.3/Ethernet Version 2 interfaces)

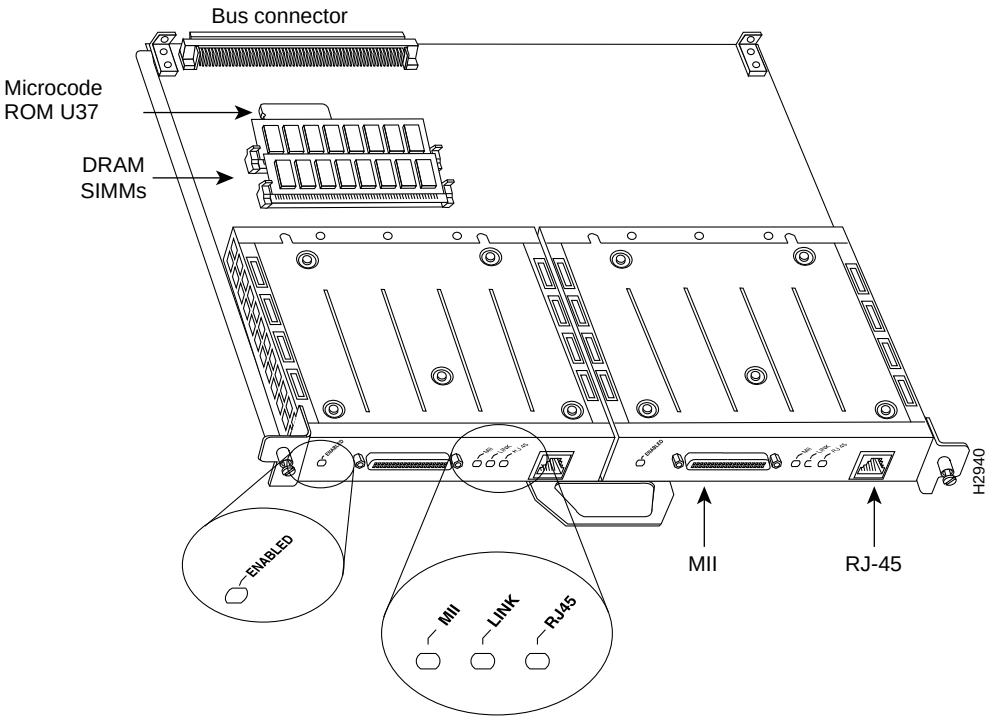
For descriptions of Ethernet transceivers and AUIs, refer to the section “Ethernet Connection Equipment” in the chapter “Preparing for Installation.” For descriptions of Ethernet network connections, refer to the section “Ethernet Connections” in the chapter “Installing the Router.”

Each port on the EIP automatically supports both Ethernet Version 1 and Version 2/IEEE 802.3 connections. When an interface is connected to an EIP port, the port automatically adjusts to the interface type. The ports are independent, so you can mix both versions on one EIP.

Fast Ethernet Interface Processor (FEIP)

The FEIP provides up to two 100-Mbps, IEEE 802.3u 100BASE-T ports. (Figure 1-12 shows a two-port FEIP.) IEEE 802.3u specifies several different physical layers for 100BASE-T: 100BASE-TX—100BASE-T half duplex, over Category 5, unshielded twisted-pair (UTP), EIA/TIA-568-compliant cable; 100BASE-FX—100BASE-T full duplex, over twisted pair or optical fiber); and 100BASE-T4—100BASE-T full duplex, using Category 3 and 4 cabling with four pairs (also called *4T+)*.

Figure 1-12 Fast Ethernet Interface Processor



Following are the product numbers associated with the FEIP:

- CX-FEIP-1TX= (interface processor with one 100BASE-TX port adapter)
- CX–FEIP-2TX= ((interface processor with two 100BASE-TX port adapters)

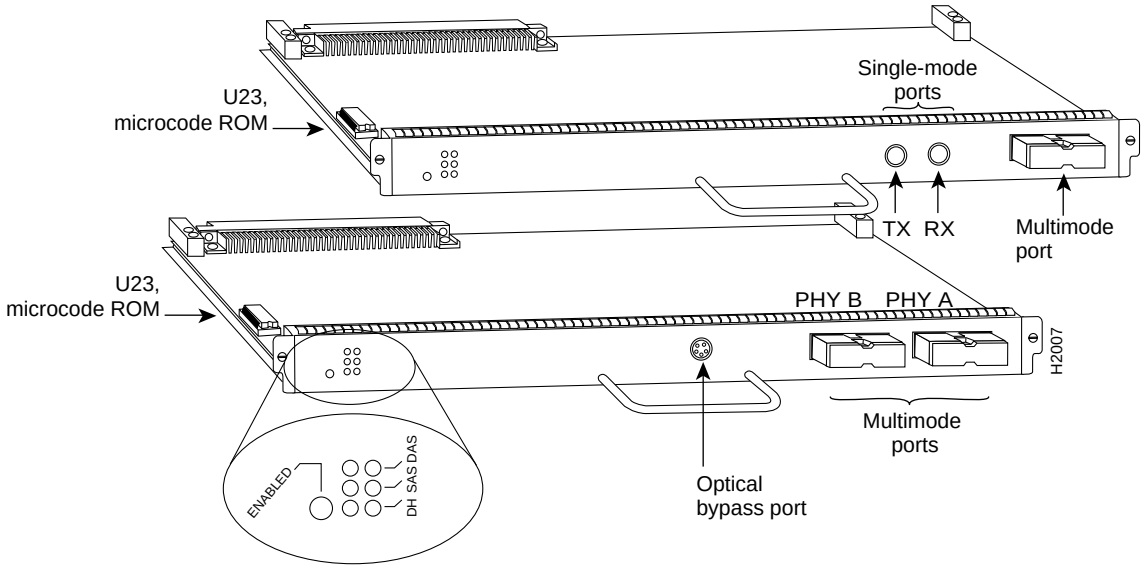
The interfaces on an FEIP can both be configured at 100 Mbps, half duplex (HDX) or full duplex (FDX), for a maximum aggregate bandwidth of 200 Mbps. The FEIP microcode boot image resides in an EPROM in socket location U37.

Fiber Distributed Data Interface Processor (FIP)

The FIP contains the industry-standard AMD SuperNet chipset for interoperability, and a 16-million instructions per second (mips) processor for high-speed (100 Mbps) interface rates. There are no restrictions on slot locations or sequence; you can install a FIP in any available interface processor slot.

Figure 1-13 shows a multimode/multimode FIP on the bottom and a single-mode/multimode FIP on the top. The FIP supports single attachment stations (SASs), dual attachment stations (DASs), dual homing, and optical bypass for both multimode and single-mode operation. The FIP complies with ANSI X3.1 and ISO 9314 FDDI standards. The default FIP microcode resides on an EPROM in socket U23.

Figure 1-13 FDDI Interface Processor



Each FIP provides a single network interface for both multimode and single-mode FDDI networks. The two FIP connectors are available in any combination of multimode (MIC) or single-mode (FC) connectors for matching multimode and single-mode fiber in the same FDDI network. Following are the product numbers associated with the FIP:

- CX-FIP-MM= (FDDI PHY-A multimode, PHY-B multimode interface processor, with an optical bypass switch mini-DIN connector)
- CX-FIP-MS= (FDDI PHY-A multimode, PHY-B single-mode interface processor)
- CX-FIP-SM= (FDDI PHY-A single-mode, PHY-B multimode interface processor)
- CX-FIP-SS= (FDDI PHY-A single-mode, PHY-B single-mode interface processor, with an optical bypass switch mini-DIN connector)
- CAB-FMDD (DIN-to-mini-DIN adapter cable for the optical bypass switch)

Each FIP provides the interface for connection to a Class A, DAS (with primary and secondary rings), or to a Class B, SAS (with only a primary ring). The multimode MIC or single-mode FC ports on the FIP provide a direct connection to the external FDDI network.

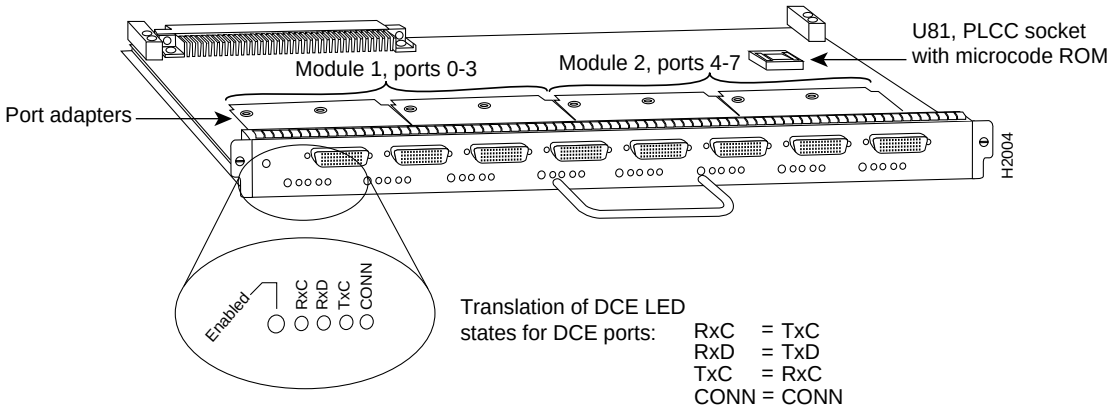
A six-pin mini-DIN connector on the multimode/multimode and single-mode/single-mode FIPs provides the connection for an optical bypass switch. When the interface is shut down, the bypass switch allows the light signal to pass directly from the receive port to the transmit port on the bypass switch, completely *bypassing* the FIP transceivers. The bypass switch does not repeat the signal, and significant signal loss may occur when transmitting to stations at maximum distances.

Optical bypass switches typically use a six-pin DIN or mini-DIN connector. A DIN-to-mini-DIN adapter cable (CAB-FMDD) is included with the FIP to allow connection to either type of connector. For a detailed description of optical bypass and FDDI connections, refer to the section "FDDI Connection Equipment" in the chapter "Preparing for Installation." For descriptions of FDDI network connections, refer to the section "FDDI Connections" in the chapter "Installing the Router."

Fast Serial Interface Processor (FSIP)

The FSIP provides four or eight channel-independent, synchronous serial ports that support full-duplex operation at T1 (1.544 Mbps) and E1 (2.048 Mbps) speeds. Each port supports any of the available interface types: EIA/TIA-232, EIA/TIA-449, V.35, X.21, EIA-530, and E1-G.703/G.704. Figure 1-14 shows an eight-port FSIP. The eight ports are divided into two four-port modules, each of which is controlled by a dedicated Motorola MC68040 processor and contains 128 kilobytes (KB) of static random-access memory (SRAM). Each module can support up to 4 T1 or 3 E1 interfaces, and an aggregate bandwidth of up to 8 Mbps at full-duplex operation. The type of electrical interface, the amount of traffic, and the types of external data service units (DSUs) connected to the ports affect actual rates. For information on setting up high-speed interfaces, refer to the section "Configuring the FSIP" in the chapter "Maintaining the Router." The default FSIP microcode resides on a PLCC-type EPROM in socket U81.

Figure 1-14 Fast Serial Interface Processor



Additional port adapters are available as spares so that you can replace one that fails; however, *you cannot upgrade a four-port FSIP to an eight-port by adding port adapters*. Each FSIP comprises an FSIP board with two or four port adapters installed. Following are the FSIP product numbers:

- CX-FSIP4=, CX-FSIP8= (four- and eight-port interface processors)
- PA-7KF-E1/75=, PA-7KF-E1/120= (two-port, 75- and 120-ohm E1-G.703/G.704 port adapters)
- PA-7KF-SPA= (two-port, universal serial port adapter)

The four-port FSIP is not constructed to support additional ports after it leaves the factory. It contains the circuitry to control only one four-port module. For port adapter descriptions, refer to "Universal Serial Port Adapters" which follows in this section.

There are no restrictions on slot locations or sequence; you can install FSIPs in any available interface processor slots. For descriptions of serial connection equipment, refer to the section "Serial Connection Equipment" in the chapter "Preparing for Installation." For examples of network connections, refer to the section "Serial Connections" in the chapter "Installing the Router."

All interface types except EIA-530 and E1-G.703/G.704 are individually configurable for operation with either external timing (DTE mode) or internal timing (DCE mode); EIA-530 operates with external timing only. In addition, all interfaces support nonreturn to zero (NRZ) and nonreturn to zero inverted (NRZI) format, and both 16-bit and 32-bit cyclic redundancy checks (CRCs). The default configuration is for NRZ format and 16-bit CRC. You can change these default settings with software commands. (See the section "Configuring the FSIP" in the chapter "Maintaining the Router.")

In order to provide a high density of ports, the FSIP uses special *port adapters* and *adapter cables*. A port adapter is a daughter card that provides the physical interface for two FSIP ports. Both ports use the same high-density, 60-pin universal receptacle that supports all interface types. The adapter cable connected to the port determines the interface type and mode.

The interface ports are not set to a default mode or for a default clock source, so there are no software commands required to enable internal or external timing (DCE or DTE). Each port automatically supports the mode of the port adapter cable when one is connected. However, there is no default clock rate set. You must set the clock rate on all DCE ports with the **clockrate** command before the port can operate with an external timing signal.

To use the port as a DCE interface, you must set the clock rate and connect a DCE adapter cable. To use the port as a DTE interface, you need only connect a DTE adapter cable to the port. If you connect a DTE cable to a port on which a clock rate is set, the system will ignore the clock rate until a DCE cable is attached. For example, you can change an interface from an EIA/TIA-232 to a V.35 by replacing the adapter cable, or change the mode of an EIA/TIA-232 DTE port by replacing the EIA/TIA-232 DTE cable with an EIA/TIA-232 DCE cable, provided that you have already specified a clock rate for the port.

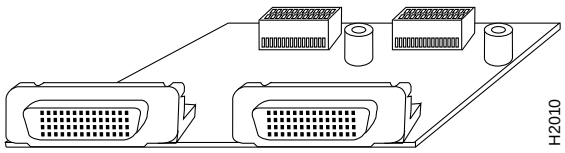
Note Although no software configuration is necessary to enable internal clocking for DCE mode, you cannot bring up a DCE interface until you set the clock rate. For a brief description of the **clockrate** command, refer to the section "Configuring the FSIP" in the chapter "Maintaining the Router." For complete command descriptions and instructions, refer to the related software documentation.

Universal Serial Port Adapters

The FSIP uses special universal serial port adapters and adapter cables to allow up to eight interface ports on an FSIP, regardless of the size or form factor of the connectors typically used with each electrical interface type. Figure 1-15 shows a universal serial port adapter with the 60-pin connectors that support all interface types. The adapter cable connected to the port determines the interface type and mode.

The universal port adapters are field-replaceable daughter cards mounted to the FSIP, and each provides two high-density connectors for two FSIP ports. (See Figure 1-15.) The 60-pin D-shell receptacle supports EIA/TIA-232, V.35, EIA/TIA-449, X.21, and EIA-530.

Figure 1-15 Universal Serial Port Adapter



The router (FSIP) end of all universal-type adapter cables is a 60-pin plug that connects to the 60-pin port (receptacle) on the FSIP. The network end of the cable is an industry-standard connector for the type of electrical interface that the cable supports: DB-25 for EIA/TIA-232 and EIA-530, DB-37 for EIA/TIA-449, DB-15 for X.21, or a standard V.35 block connector. For most interface types, the adapter cable for DTE mode uses a plug at the network end, and the cable for DCE mode uses a receptacle at the network end. However, V.35 adapter cables are available with either a V.35 plug or a receptacle for either mode, and EIA-530 is available only in DTE mode with a DB-25 plug.

Factory-installed 4-40 thumbscrews are standard at the network end of all cable types except V.35. A metric conversion kit with M3 thumbscrews is included with each cable to allow connection to devices that use metric hardware.

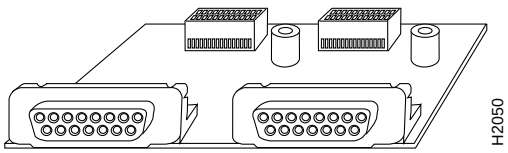
The FSIP is shipped from the factory with two or four dual-port adapters installed. Additional port adapters are available as spares so that you can replace one that fails; however, *you cannot upgrade a four-port FSIP to an eight-port by adding port adapters*. The four-port FSIP is manufactured with only one four-port module and processor.

For port adapter replacement instructions, refer to the section “Configuring the FSIP” in the chapter “Maintaining the Router.” The appendix “Cabling Specifications” provides adapter cable pinouts. However, because the FSIP uses a special high-density port that requires special adapter cables for each electrical interface type, we recommend that you obtain serial interface cables from the factory.

E1-G.703/G.704 Port Adapter

The FSIP E1-G.703/G.704 port adapter (see Figure 1-16) connects the Cisco 7507 with 2-Mbps leased-line services. The interface eliminates the need for a separate, external data termination unit to convert a standard serial interface (such as V.35) to a G.703/G.704/G.732 interface.

Figure 1-16 FSIP E1-G.703/G.704 Port Adapter



The FSIP can be configured to support up to eight E1-G.703/G.704 ports (four ports per module, two modules per FSIP). FSIP bandwidth can be allocated by the user, and the maximum aggregate bandwidth per four-port module is 16 Mbps, full duplex. We recommend that you leave one port on each module shut down to avoid exceeding this 16-Mbps maximum per module. Each of the four interfaces can operate up to 2.048 Mbps, which potentially presents a load greater than 16 Mbps, full duplex, if all four interfaces are configured. Eight E1-G.703/G.704 ports can be supported up to the 16-Mbps aggregate bandwidth capability; however, it is not possible to simultaneously support eight E1-G703/G.704 ports at 100-percent peak bandwidth utilization, without exceeding the 16-Mbps maximum per module.

Two versions of the E1-G.703/G.704 interface are available: one supports balanced mode, and the other supports unbalanced mode. Neither the modes nor the cables are interchangeable; you cannot configure a balanced port to support an unbalanced line, nor can you attach an interface cable intended for a balanced port to an unbalanced port.

The FSIP E1-G.703/G.704 interface supports both framed and unframed modes of operation, a loopback test, and a four-bit CRC. The interface can operate with either a line-recovered or an internal clock signal. The FSIP is configured at the factory with from one to four E1-G.703/G.704 port adapters. Each port adapter provides two 15-pin D-shell (DB-15) receptacles, which support only E1-G.703/G.704 interfaces.

The FSIP E1-G.703/G.704 interface uses a DB-15 receptacle for both the balanced and unbalanced ports. The label adjacent to the port indicates whether the port is balanced or unbalanced; you must connect the correct type of interface cable or the port will not operate.

The FSIP end of all E1-G.703/G.704 adapter cables is a DB-15 connector. At the network end, the adapter cable for unbalanced connections uses a BNC connector. The adapter cables for balanced mode are available with several connector types to accommodate connection standards in different countries. You must use the proprietary cables to connect the E1-G.703/G.704 port to your network.

Cables for balanced and unbalanced mode are available with the following types of network-end connectors:

- Balanced (120-ohm) twinax split at the network end, with separate transmit and receive cables, each with a BNC connector
- Balanced (120-ohm) cable with a DB-15 connector at the network end
- Unbalanced (75-ohm) coax with BNC connectors at the network end (used primarily for connection in the United Kingdom)

In addition, some connections require bare-wire connections (directly to terminal posts).

Table 1-3 lists the model numbers and descriptions of the E1-G.703/G.704 port adapters and cables.

Table 1-3 Model Numbers and Descriptions of E1-G.703/G.704 Port Adapter and Cables

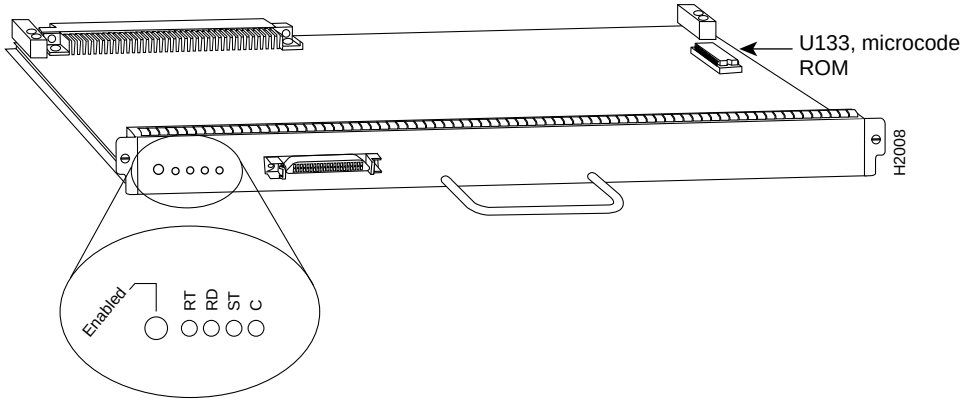
Port Adapter and Cable Model Numbers	Description
PA-7KF-E1/120=[1]	Dual-port E1-G.703/G.704 120 ohm, balanced
PA-7KF-E1/75=	Dual-port E1-G.703/G.704 75 ohm, unbalanced
CAB-E1-TWINAX=	E1 cable twinax 120 ohm, balanced, 5 m
CAB-E1-DB15=	E1 cable, DB-15, 120 ohm, balanced, 5 m
CAB-E1-BNC=	E1 cable BNC 75 ohm, unbalanced, 5 m

1. The appended equal sign (=) indicates a spare part.

HSSI Interface Processor (HIP)

The HIP, shown in Figure 1-17, provides a full-duplex, synchronous serial interface for transmitting and receiving data at rates of up to 52 Mbps. HSSI, recently standardized as EIA/TIA-612/613, provides access to services at T3 (45 Mbps), E3 (34 Mbps), and SONET STS-1 (51.82 Mbps) rates. The actual rate of the interface depends on the external DSU and the type of service to which it is connected. The default HIP microcode resides on an EPROM in socket U133.

Figure 1-17 HSSI Interface Processor



The HIP interface port is a 50-pin, SCSI-II-*type* receptacle; however, you need an HSSI interface cable to connect the HIP with an external DSU.

Note Although the HSSI port and cable are physically similar to SCSI-II format, the HSSI specification is more stringent than that for SCSI-II, and we cannot guarantee reliable operation if a SCSI-II cable is used.

A null modem cable allows you to connect two collocated routers back to back to verify the operation of the HSSI interface or to build a larger node by linking the routers directly. For a description of HSSI network and null modem connections, refer to the section “HSSI Connections” in the chapter “Installing the Router.” The appendix “Cabling Specifications” provides connector pinouts and cable assembly drawings.

Following are the product numbers associated with the HIP:

- CX-HIP= (single-port HSSI interface processor
- CAB-HSI1= (straight-through HSSI cable)
- CAB-HNUL= (null-modem HSSI cable)

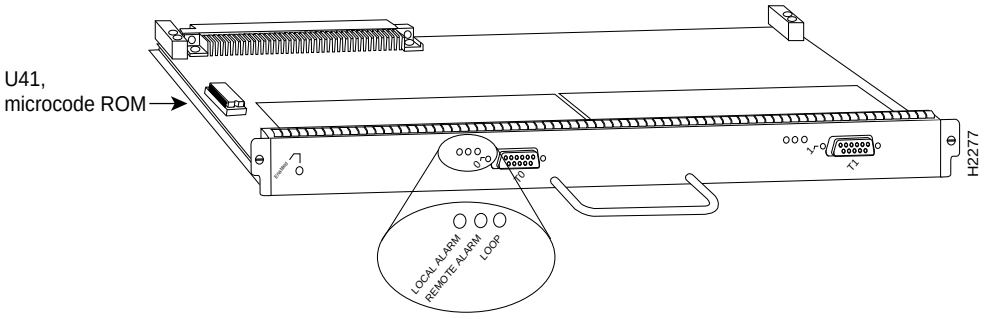
There are no restrictions on slot locations or sequence; you can install a HIP in any available interface processor slot.

MultiChannel Interface Processor (MIP)

The MIP provides up to two channelized T1 or E1 connections via serial cables to a CSU. On the MIP, two controllers can each provide up to 24 T1 channel-groups or 30 E1 channel-groups. Each channel-group is presented to the system as a serial interface that can be configured individually.

The MIP, shown in Figure 1-18, provides one or two controllers for transmitting and receiving data bidirectionally at the T1 rate of 1.544 Mbps or one or two controllers for transmitting and receiving data bidirectionally at the E1 rate of 2.048 Mbps. For wide-area networking, the MIP can function as a concentrator for a remote site. The default MIP microcode resides on an EPROM in socket U41.

Figure 1-18 Multichannel Interface Processor (Dual-Port Module Shown)



Following are the product numbers associated with the MIP:

- CX-MIP-1CT1= (one-port, T1interface processor)
- CX-MIP-2CT1= (two-port, T1 interface processor)
- CX-MIP-1CE1/75= (one-port interface processor with a 75-ohm, E1 port adapter)
- CX-MIP-2CE1/75= (two-port interface processor with 75-ohm, E1 port adapters)
- CX-MIP-1CE1/120= (one-port interface processor with a 120-ohm, E1 port adapter)
- CX-MIP-2CE1/120= (two-port interface processor with 120-ohm, E1 port adapters)

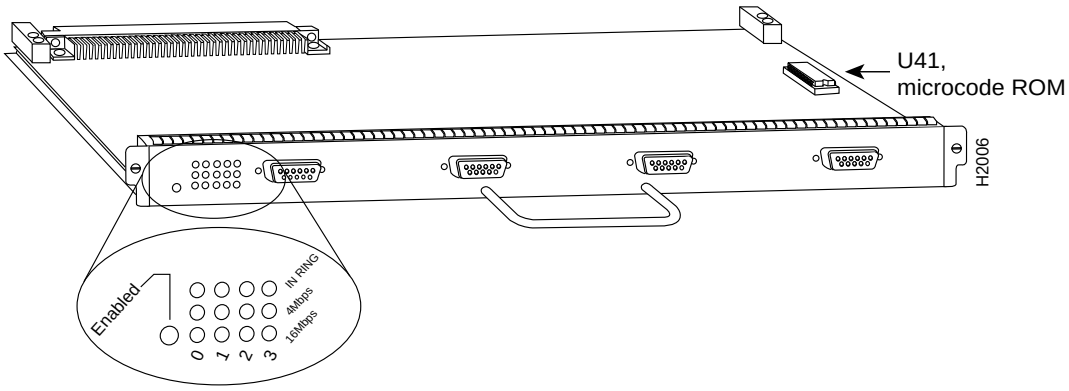
There are no restrictions on slot locations or sequence; you can install a MIP in any available interface processor slot.

Note The MultiChannel Interface Processor (MIP) and the Channel Attachment Interface Processor (CIP) use entirely dissimilar interfaces and have entirely dissimilar functions within the Cisco 7507.

Token Ring Interface Processor (TRIP)

The TRIP, shown in Figure 1-19, provides two or four Token Ring ports for interconnection with IEEE-802.5 and IBM Token Ring media. The TRIP uses the IBM 16/4-Mbps chipset with an imbedded, performance-enhanced interface driver and a 16.7-MHz bit-slice processor for high-speed processing. The speed on each port is independently software-configurable for either 4 or 16 Mbps. The default TRIP microcode resides on an EPROM in socket U41.

Figure 1-19 Token Ring Interface Processor



The TRIP is available with two or four ports. Each port requires a media access unit (MAU) to connect the DB-9 TRIP connectors to the external Token Ring networks. There are no restrictions on slot locations or sequence; you can install a TRIP in any available interface processor slot.

Following are the product numbers associated with the TRIP:

- CX-TRIP2= (interface processor with two IEEE 802.5 Token Ring interfaces)
- CX-TRIP4= (interface processor with four IEEE 802.5 Token Ring interfaces)

For descriptions of Token Ring connectors and MAUs, refer to the section “Token Ring Connection Equipment” in the chapter “Preparing for Installation.” For descriptions of Token Ring network connections, refer to the section “Token Ring Connections” in the chapter “Installing the Router.”

Functional Overview

This section describes functions that support the router's high availability and maintainability. OIR for interface processors and redundant hot-swap for power supplies enable you to quickly install new equipment without interrupting system power or shutting down interfaces. The environmental monitoring and reporting functions continuously monitor temperature and voltage points in the system, and provide reports and warning messages that enable you to quickly locate and resolve problems and maintain uninterrupted operation. The redundant power option provides dual load-sharing power supplies. In the event of a power supply failure, or if one of two separate power sources fails, the redundant power option assures uninterrupted operation.

Addresses and Port Numbers

Each interface (port) in a Cisco 7507 uses different types of addressing. The *slot/port number* is the actual physical location of the interface connector (port) within the chassis (slot). The system software uses the slot/port numbers to control activity within the router and to display status information. These slot/port numbers are not used by other devices in the network; they are specific to the individual router and its internal components and software.

The Media Access Control (MAC) layer or *hardware* address is a standardized data link layer address that is required for every port or device that connects to a network. The Cisco 7507 uses a specific method to assign and control the MAC-layer addresses of its interfaces.

The following sections describe how the Cisco 7507 assigns and controls both the slot/port numbers and MAC–layer addresses for interfaces within the chassis.

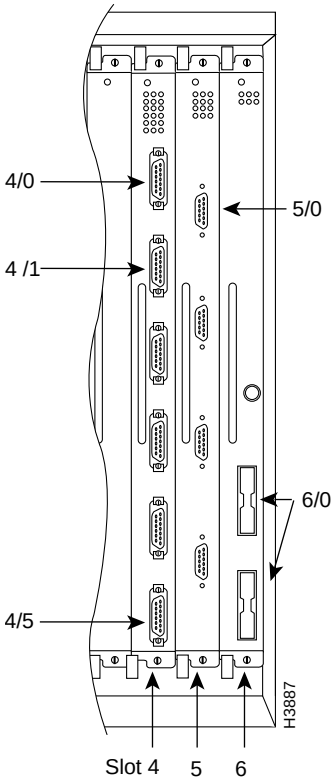
Slot/Port Numbers

In the Cisco 7507, slot/port numbers specify the actual location of each interface port on the router interface processors. (See Figure 1-20.) The number uses the format *slot*/*port*. The first number identifies the slot in which the interface processor is installed (0 through 6, beginning at the far left slot). The second number identifies the port number on the interface processor. The ports on each interface processor are numbered sequentially from *top* to *bottom* beginning with the port 0.

Interface ports maintain the same slot/port number regardless of whether other interface processors are installed or removed. However, when you move an interface processor to a different slot, the first number changes to reflect the new slot number. For example, on a six-port EIP in slot 0, the slot/port number of the first (top) port is 0/0 and that of the last (bottom) port is 0/5. If you remove the EIP from slot 0 and install it in slot 1, the slot/port numbers of those same ports become 1/0 and 1/5, respectively.

Figure 1-20 shows some of the slot/port numbers of a sample system.

Figure 1-20 Interface Slot/Port Number Examples (Slots 4, 5, and 6 Shown)



Interface slots are numbered 0 and 1, and 4 through 6 from left to right. The port numbers always begin at 0 and are numbered from top to bottom. The number of additional ports depends on the number of ports available on an interface. For example, FDDI interfaces are always /0, because each FIP supports one interface. (The multiple connectors on the FIP can be misleading, but they provide multiple attachment options for a *single* FDDI interface.) Ethernet interfaces can be numbered from /0 through /5 because EIPs support up to six Ethernet ports. Serial interfaces on an eight-port FSIP are numbered /0 through /7, and so forth.

You can identify interface ports by physically checking the slot/port number on the back of the router or by using software commands to display information about a specific interface or all interfaces in the router. To display information about every interface, use the **show interface** command without arguments. To display information about a specific interface, use the **show interface** command with the interface type and slot/port number in the format **show interface** [*type slot/port*]. If you abbreviate the command (**sho int**) and do not include arguments, the system interprets the command as **show interface** and displays the status of all interfaces.

Following is an example of how the **show interface** command, used without arguments, displays status information (including the physical slot/port number) for each interface in the router. In the following example, most of the status information for each interface is omitted.

```
Router# sh int

Serial0/0 is up, line protocol is up
  Hardware is cxBus Serial
  Internet address is 1.1.1.4, subnet mask is 255.255.255.0
  (display text omitted)
Ethernet1/2 is up, line protocol is up
  Hardware is cxBus Ethernet, address is 0000.0c02.d0f1 (bia 0000.0c02.d0f1)
  (display text omitted)
Fddi4/0 is administratively down, line protocol is down
  Hardware is cxBus Fddi, address is 0000.0c02.adc2 (bia 0000.0c02.adc2)
  Internet address is 1.1.1.8, subnet mask is 255.255.255.0
  (display text omitted)
```

You can also use arguments such as the interface type (**ethernet**, **tokenring**, **fddi**, **serial**, **hssi**, and so forth) and the port address (slot/port) to display information about a specific interface only.

The following example shows the display for the first (far left) Ethernet port on an EIP in slot 1:

```
Router# sh int ether 1/0

Ethernet1/0 is up, line protocol is up
  Hardware is cxBus Ethernet, address is 0000.0c02.d0ce (bia 0000.0c02.d0ce)
  Internet address is 1.1.1.3, subnet mask is 255.255.255.0
  MTU 1500 bytes, BW 10000 Kbit, DLY 1000 usec, rely 255/255, load 1/255
  Encapsulation ARPA, loopback not set, keepalive set (10 sec)
  (display text omitted)
```

For complete command descriptions and instructions, refer to the *Router Products Configuration Guide* and *Router Products Command Reference* publications.

MAC-Layer Address Allocator

All network interface connections (ports), except serial ports, require a unique MAC address, which is also known as a *hardware* address. Typically, the MAC address of an interface is stored on a memory component that resides directly on the interface circuitry; however, the OIR feature requires a different method.

The OIR feature allows you to remove an interface processor and replace it with another identically configured one. If the new interfaces match the interfaces you removed, the system immediately brings them on line. In order to allow OIR, an address allocator with unique MAC addresses is stored in a memory device on the backplane. Each address is reserved for a specific slot/port in the router regardless of whether an interface resides in that port. The MAC addresses are assigned to the ports in sequence; the first address is assigned to the first port on the interface processor in slot 0 and the last address is assigned to the last port on the interface processor in slot 3. This address scheme allows you to remove interface processors and insert them into other routers without causing the MAC addresses to move around the network or be assigned to multiple devices.

Note that if the MAC addresses were stored on each interface processor, OIR would not function because you could never replace one interface with an identical one; the MAC addresses would always be different. Also, each time an interface was replaced, other devices on the network would have to update their data structures with the new address, and, if they did not do so quickly enough, could cause the same MAC address to appear in more than one device at the same time.

Storing the MAC addresses in a memory device on the backplane avoids these problems. When an interface is replaced with another identical interface, there is no need for other devices in the network to update their data structures and routing tables.

Note Storing the MAC addresses for every port in one central location means they stay with the memory device on which they are stored.

Online Insertion and Removal (OIR)

The OIR function allows you to install and replace interface processors while the system is operating; you do not need to notify the software or shut down the system power. All interface processors support online insertion and removal. The following is a functional description of OIR for background information only; for specific procedures for installing and replacing interface processors on line, refer to the sections “Removing Interface Processors” and “Installing Interface Processors” in the chapter “Maintaining the Router.”

Caution All interface processors support OIR. The RSP2 is a required system component that cannot be removed if the system is operating. Removing an RSP2 while the system is operating will cause the system to shut down or crash and might damage or destroy memory files.

Each interface processor contains a bus connector with which it connects to the system backplane. Each card connector comprises a set of tiered pins in three lengths. The pins send specific signals to the system as they make contact with the backplane. The system assesses the signals it receives and the order in which it receives them to determine what event is occurring and what task it needs to perform, such as reinitializing new interfaces or shutting down removed ones. For example, when inserting an interface processor, the longest pins make contact with the backplane first, and the shortest pins make contact last. The system recognizes the signals and the sequence in which it receives them. The system expects to receive signals from the individual pins in this logical sequence, and the ejectors help to ensure that the pins mate in this sequence.

When you remove or insert an interface processor, the backplane pins send signals to notify the system, which then performs as follows:

1. Rapidly scans the backplane for configuration changes.
2. Initializes all newly inserted interface processors, noting any removed interfaces and placing them in the administratively shut down state.
3. Brings all previously configured interfaces on the interface processor back to the state they were in when they were removed. Any newly inserted interfaces are put in the administratively shut-down state, as if they were present (but unconfigured) at boot time. If a similar interface processor type has been reinserted into a slot, then its ports are configured and brought on line up to the port count of the original interface processor.

OIR functionality enables you to add, remove, or replace interface processors while the system is on line. This provides a method that is seamless to end users on the network, maintains all routing information, and ensures session preservation.

When you insert a new interface processor, the system runs a diagnostic on the new interfaces and compares them to the existing configuration. If this initial diagnostic fails, the system remains off line for another 15 seconds while it performs a second set of diagnostics to determine whether or not the interface processor is faulty and if normal system operation is possible.

If the second diagnostic test passes, which indicates that the system is operating normally and the new interface processor is faulty, the system resumes normal operation but leaves the new interfaces disabled.

If the second diagnostic fails, the system crashes, which usually indicates that the new interface processor has created a problem in the bus and should be removed.

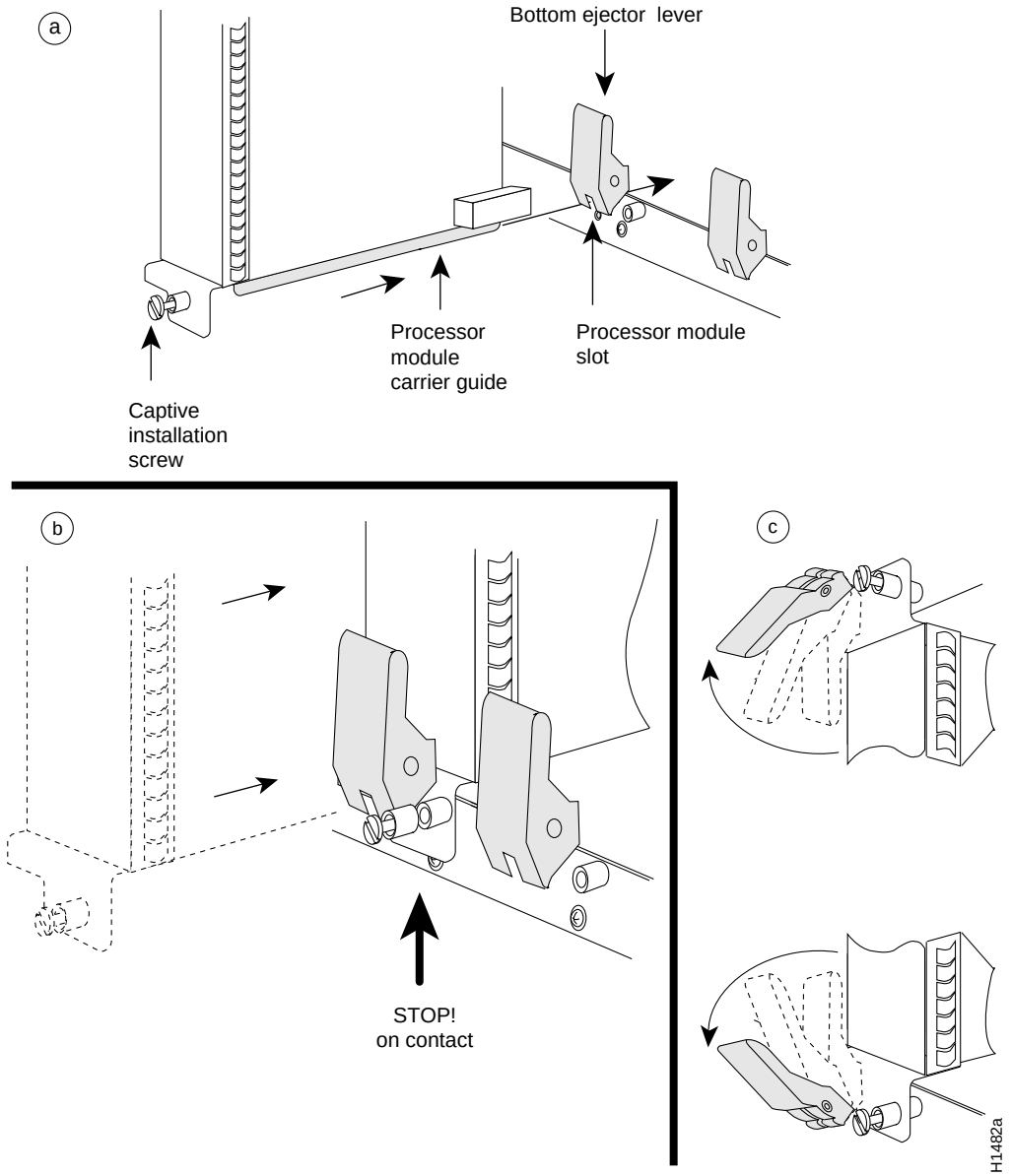
The system brings on line only interfaces that match the current configuration and were previously configured on line; all others require that you configure them with the **configure** command. On interface processors with multiple interfaces, only the interfaces already configured are brought on line. For example, if you replace an EIP-4 with an EIP-6, only the four previously configured interfaces (ports /0 through /3) are brought on line; the last two remain in the down state until you configure them and bring them on line.

The function of the ejector levers (see Figure 1-21) is to align and seat the card connectors in the backplane. Failure to use the ejectors and insert the interface processor properly can disrupt the order in which the pins make contact with the backplane. Following are examples of incorrect insertion practices and results:

- Using the handle to force an interface processor all the way into the slot can pop the ejectors out of their springs. If you then try to use the ejectors to seat the interface processor, the first layer of pins (which are already mated to the backplane) can disconnect and then remate with the backplane, which the system interprets as a board failure.
- Using the handle to force or slam an interface processor all the way into the slot can also damage the pins on the board connectors if they are not aligned properly with the backplane.
- When using the handle (rather than the ejectors) to seat an interface processor in the backplane, you may need to pull the interface processor back out and push it in again to align it properly. Even if the connector pins are not damaged, the pins mating with and disconnecting from the backplane will cause the system to interpret a board failure. Using the ejectors ensures that the board connector mates with the backplane in one continuous movement.
- Using the handle to insert or remove an interface processor, or failing to push the ejectors to the full 90-degree position, can leave some (not all) of the connector pins mated to the backplane, a state which will hang the system. Using the ejectors and making sure that they are pushed fully into position ensures that all three layers of pins are mated with (or free from) the backplane.

It is also important to use the ejector levers when removing an interface processor to ensure that the board connector pins disconnect from the backplane in the logical sequence expected by the system. Any interface processor that is only partially connected to the backplane can hang the bus.

Figure 1-21 Ejector Levers and Captive Installation Screws



Microcode

The Cisco 7507 supports downloadable microcode for most upgrades, which enables you to load new microcode images into Flash memory instead of replacing the microcode ROMs on the boards. The latest microcode version for each interface processor type is bundled with the system software image. New microcode images are now distributed on floppy disk as part of a software maintenance release; microcode upgrades are no longer distributed individually.

Note We strongly recommend that the microcode bundled with the system software be used as a package. Overriding the bundle could possibly result in incompatibility between the various interface processors in the system.

The default operation is to load the microcode from the bundled image. At system startup, an internal system utility scans for compatibility problems between the installed interface processor types and the bundled microcode images, then decompresses the images into running memory (DRAM). The bundled microcode images then function the same as images loaded from the individual microcode ROMs on the processor modules. You can override the default and instruct the system to load a specific microcode image from a Flash memory file or from the microcode ROM with the **microcode** [*card type*] **flash** [*file name*] command.

The **show microcode** command lists all of the microcode images that are bundled with the system software image. In order to support online insertion and replacement (OIR), the system loads a microcode image for all available processor types.

Following is an example of the **show microcode** command (microcode versions are examples only):

```
Router# show microcode
Microcode bundled in system

Card    Microcode    Target Hardware    Description
Type    Version      Version
----    ---------    ---------------    -----------
EIP      10.1              1.x          EIP version 10.1
FIP      10.2              2.x          FIP version 10.2
TRIP     10.1              1.x          TRIP version 10.1
AIP      10.5              1.x          AIP version 10.5
FEIP     10.1              1.x          FEIP version 10.1
FSIP     10.6              1.x          FSIP version 10.6
HIP      10.2              1.x          HIP version 10.2
MIP      11.0              1.x          MIP version 11.0
CIP      10.3              1.x          CIP version 10.3

Router#
```

The microcode version and description lists the bundled microcode version for each processor type, which is not necessarily the version that is currently loaded and running in the system. A microcode image that is loaded from ROM or a Flash memory file is not shown in this display. To display the currently loaded and running microcode version for each processor type, issue the **show controller cybus** command.

The target hardware version lists the minimum hardware revision required to ensure compatibility with the new software and microcode images. When you load and boot from a new bundled image, the system checks the hardware version of each processor module that it finds installed and compares the actual version to its target list.

If the target hardware version is different from the actual hardware version, a warning message appears when you boot the router, indicating that there is a disparity between the target hardware and the actual hardware. You will still be able to load the new image; however, contact a customer service representative for information about upgrades and future compatibility requirements.

To display the current microcode version for each interface processor, enter the **show controller cybus** command. The following example shows an FSIP running Microcode Version 10.0:

```
Router# show cont cybus

  (display text omitted)
FSIP 0, hardware version 4, microcode version 10.0
  (display text omitted)
```

Although most microcode upgrades are distributed on floppy disk, some exceptions may require microcode EPROM replacement. If so, refer to the section "Microcode Component Replacement" in the chapter "Maintaining the Router" for EPROM replacement procedures. (Instructions are also provided with the upgrade kit.) For complete command descriptions and instructions, refer to the related software documentation.

Redundant Power

One 700W, AC-input or DC-input power supply is standard in the router. A second, *identical* power supply can be installed to provide redundant power. Dual power supplies are load sharing; when two power supplies are installed and both are operational (both are turned on), each concurrently provides about half of the required power to the system. If one of the power supplies fails, the second power supply ramps up to full power to maintain uninterrupted system operation. Dual power supplies should be connected to separate input lines so that, in case of a line failure, the second source will most likely still be available. Load sharing and redundancy are automatically enabled when the second power supply is installed; no software configuration is required.

Caution To prevent problems, do *not* mix DC-input and AC-input power supplies in the same chassis. Your Cisco 7507 must have *either* DC-input or AC-input power supplies.

Environmental Monitoring and Reporting Functions

The environmental monitoring and reporting functions, controlled by the chassis interface board, enable you to maintain normal system operation by identifying and resolving adverse conditions prior to loss of operation. The environmental monitoring functions constantly monitor the internal chassis air temperature and DC supply voltages. Each power supply monitors its own voltage and temperature and shuts itself down if it detects a critical condition within the power supply. If conditions reach shutdown thresholds, the system shuts down to avoid equipment damage from excessive heat. The reporting functions periodically log the values of measured parameters so that you can retrieve them for analysis later, and the reporting functions display warnings on the console if any of the monitored parameters exceed defined thresholds.

In addition to monitoring internal temperature and voltage levels, the system also monitors the blower. If the blower fails, the system displays a warning message on the console. If the blower is still not operating properly after two minutes, the system shuts down to protect the internal components against damage from excessive heat.

Environmental Monitoring

Three sensors on the RSP2 monitor the temperature of the cooling air that flows through the processor slots: inlet, hotpoint, and exhaust. The sensors are located at the bottom, center, and top of the RSP2, when facing the interface processor end of the chassis and viewing the RSP2 as it is installed.

The power supply uses the Normal, Critical, and Warning levels to monitor DC voltages. Table 1-4 lists temperature thresholds for the three processor-monitored levels. Table 1-5 lists the DC power thresholds for the Normal and Critical (power supply-monitored) levels.

Table 1-4 Typical Processor-Monitored Temperature Thresholds

Parameter	Normal	High Warning	High Critical	Shutdown
Inlet	10–40 C	44 C	50 C	–
Hotpoint	10–40 C	54 C	60 C	–
Exhaust	10–40 C	–	–	–
Processors	–	–	–	70 C
Power supply	–	–	–	75 C
Restart	40 C	–	–	–

Table 1-5 Typical Power Supply-Monitored DC-Voltage Thresholds

Parameter	Normal	Low Critical	Low Warning	High Warning	High Critical
+5V	4.74 to 5.26	4.61	4.94	5.46	5.70
+12V	10.20 to 13.8	10.90	11.61	12.82	13.38
–12V	–10.20 to –13.80	–10.15	–10.76	–13.25	–13.86
+24V	20.00 to 28.00	20.38	21.51	26.42	27.65

- Normal—All monitored parameters are within normal tolerances.
- Warning (low and high)—The system is approaching an out-of-tolerance condition. The system will continue to operate, but operator monitoring or action is recommended to bring the system back to a normal state.
- Critical (low and high)—An out-of-tolerance temperature or voltage condition exists. The system may not continue operation. If a voltage measurement reaches this level, the power supply can shut down the system. If the blower fails, the system will display a warning message and shut down in two minutes. Immediate operator action is required.
- Processor shutdown—The chassis interface has detected a temperature or blower-failure condition that could result in physical damage to system components and has disabled DC power to all interface processors (in slots 0 through 1 and 4 through 6). DC power to the RSP2, chassis interface, and blower stays on, but no RSP2-related processing takes place. Immediate operator action is required. DC power remains off until the inside temperature of the chassis reaches 40 C (104 F), at which point the system will restart up to 15 times (if required). If the source of the shutdown has not been corrected, the system will execute a hard shutdown. Before any shutdown, the system logs the status of monitored parameters in NVRAM so that you can retrieve it later to help determine the cause of the problem.

- Power supply shutdown—An out-of-tolerance voltage, current, or temperature condition was detected within the power supply and it was shut down (or a shutdown is imminent). All DC power remains disabled until the operator toggles the power switch and corrects the problem that caused the shutdown (if any). This condition is typically because of one of the following reasons:
  - Loss of AC or DC input power (the power source failed).
  - Power supply detected an overvoltage, overcurrent, AC or DC undervoltage, or overtemperature condition within the power supply. This includes operator shutdown by turning off the system power switch, which the power supply interprets as an undervoltage condition.
  - The chassis interface detected an overtemperature condition within the system.

If the air temperature exceeds a defined threshold, the system processor displays warning messages on the console terminal and, if the temperature exceeds the shutdown threshold, it shuts down the system. The system stores the present parameter measurements for both temperature and DC voltage in NVRAM, so that you can retrieve it later as a report of the last shutdown parameters.

The power supplies monitor internal power supply temperature and voltages. A power supply is either within tolerance (Normal) or out of tolerance (Critical or Warning levels), as shown in Table 1-5. If an internal power supply temperature or voltage reaches a critical level, the power supply shuts down without any interaction with the system processor.

If the system detects that AC or DC input power is dropping, but it is able to recover before the power supply shuts down, it logs the event as an intermittent power failure. The reporting functions display the cumulative number of intermittent power failures logged since the last power up.

Environmental Reports

The system displays warning messages on the console if chassis interface-monitored parameters exceed a desired threshold or if a blower failure occurs. You can also retrieve and display environmental status reports with the **show environment**, **show environment all**, **show environment last** and **show environment table** commands. Parameters are measured and reporting functions are updated every 60 seconds. A brief description of each of these commands follows.

Caution To prevent overheating the chassis, ensure that your system is drawing cool inlet air. Overtemperature conditions can occur if the system is drawing in the exhaust air of other equipment. Ensure adequate clearance around the sides of the chassis so that cooling air can flow through the chassis interior unimpeded. Obstructing or blocking the chassis sides will restrict the airflow and can cause the internal chassis temperature to exceed acceptable limits.

The **show environment** command display reports the current environmental status of the system. The report displays parameters that are out of the normal values. No parameters are displayed if the system status is normal. The example that follows shows the display for a system in which all monitored parameters are within Normal range. Following is sample output of the **show env** command:

```
Router# show env

All measured values are normal
```

If the environmental status is *not* normal, the system reports the worst-case status level in the last line of the display.

The **show environment last** command retrieves and displays the NVRAM log showing the reason for the last shutdown (if the shutdown was related to voltage or temperature) and the environmental status at that time. Air temperature is measured and displayed, and the DC voltages supplied by the power supply are also displayed. Following is sample output of the **show env last** command:

```
Router# show env last

  RSP(2) Inlet       previously measured at 27C/80F
  RSP(2) Hotpoint    previously measured at 38C/100F
  RSP(2) Exhaust     previously measured at 31C/87F
  +12 Voltage        previously measured at 12.17
  +5 Voltage         previously measured at 5.19
  -12 Voltage        previously measured at -12.17
  +24 Voltage        previously measured at 23.40
```

The **show environment table** command displays the temperature and voltage thresholds for each of the three RSP2 temperature sensors, for each monitored status level: low critical, low warning, high warning, and high critical, which are the same as those listed in Tables 1-4 and 1-5. The slots in which the RSP2 can be installed are indicated in parentheses (2 and 3). Also listed are the shutdown thresholds for the processor boards and power supplies. Following is sample output of the **show env table** command:

```
Router# show env table

Sample Point      LowCritical    LowWarning     HighWarning    HighCritical

RSP(2) Inlet                                    44C/111F        50C/122F
RSP(2) Hotpoint                                 54C/129F        60C/140F
RSP(2) Exhaust                                  101C/213F       101C/213C
RSP(3) Inlet                                    44C/111F        50C/122F
RSP(3) Hotpoint                                 54C/129F        60C/140F
RSP(3) Exhaust                                  101C/213F       101C/213F
+12 Voltage       10.90          11.61          12.82           13.38
+5 Voltage      4.49           4.74           5.25           5.52
-12 Voltage     -10.15         -10.76         -13.25         -13.86
+24 Voltage     19.06          21.51          26.51          28.87
Shutdown boards at           101C/213F
Shutdown power supplies at   101C/213F
```

Note Temperature ranges and values are subject to change.

The **show environment all** command displays an extended report that includes the arbiter type, backplane type, power supply type (AC or DC), wattage and status, the number and type of intermittent power failures (if any) since the system was last powered on, and the currently measured values at the RSP2 temperature sensors and the power supply voltages. The **show environment all** command also displays a report showing which slots in the Cisco 7507 are occupied (indicated by an X) and which are empty.

Active fault conditions are indicated when the blower or power supply has failed or is not present (as "Blower #3" indicates in the following example). The system expects to see one blower in the Cisco 7507, the main system blower. The system blower is designated *#1*. The active fault condition in the following example shows that there is no power supply installed in power bay B because the display indicates that power supply #2 (in the upper bay) is removed.

There are four active trip points: *restart OK*, *temperature warning*, *board shutdown*, and *power supply shutdown*. (There are no active trip points shown in the following example.) The *soft shutdowns* refer to the number of times the system will reset itself before it executes a complete chassis (or hard) shutdown.

The current temperature measurements at the three RSP2 sensors are displayed as *inlet*, *hotpoint*, and *exhaust*. The shutdown temperature source is the *hotpoint* sensor, which is located toward the center of the RSP2. System voltage measurements are also displayed, followed by the system current measurements and power supply wattage calculation. Following is sample output of the **show env all** command:

```
Router# show env all

Arbiter type 1, backplane type 7507 (id 4)
Power supply #1 is removed (id 3), power supply #2 is 700W (id 2)
Active fault conditions: none
Active trip points: Restart_Inhibit
15 of 15 soft shutdowns remaining before hard shutdown


           0123456
Dbus slots: XX XXX

         inlet        hotpoint     exhaust
RSP(3)   16C/60F       24C/71F       20C/68F

Shutdown temperature source is 'hotpoint' slot3 (requested slot2)

+12V measured at 11.84
 +5V measured at 5.05
-12V measured at -11.84
+24V measured at 23.78
+2.5 reference is 2.46

PS1 +5V Current    measured at 42.35 A (capacity 200 A)
PS1 +12V Current   measured at 6.86 A (capacity 35 A)
PS1 -12V Current   measured at 0.55 A (capacity 3 A)
PS1 output is 296 W
```