CHAPTER 1

Product Overview

The 5-slot, Cisco 7505 router provides high reliability, availability, serviceability, port density, and performance. The Cisco 7505 supports multiprotocol, multimedia routing and bridging with a wide variety of protocols and any combination of Ethernet, Token Ring, Fiber Distributed Data Interface (FDDI), serial, High-Speed Serial Interface (HSSI), multichannel applications, and channel attachment media. All network interfaces reside on processors called *interface processors*, which provide a direct connection between the high-speed CyBus and the external networks.

Online insertion and removal (OIR) allows you to add, replace, or remove interface processors without interrupting the system power or entering any console commands. Environmental monitoring and reporting functions enable you to maintain normal system operation by resolving adverse environmental conditions prior to loss of operation. If conditions reach critical thresholds, the system shuts down to avoid equipment damage from excessive heat or electrical current. Downloadable software and microcode allows you to load new images into Flash memory remotely, without having to physically access the router, for fast, reliable upgrades.

This chapter provides physical and functional overviews to familiarize you with your new router. It contains physical descriptions of the system hardware and major components, and functional descriptions of hardware-related features. Descriptions and examples of software commands appear only when they are necessary for installing or maintaining the system hardware.

Following is a list of acronyms that identify the system components and features:

- AIP—Asynchronous Transfer Mode (ATM) Interface Processor
- CIP—Channel Interface Processor
- CxBus—Cisco Extended Bus, 533-megabit-per-second (Mbps) data bus for processor modules used in the Cisco 7000 series routers
- CyBus—Cisco Extended Bus, 1.067-gigabit-per-second (Gbps) data bus for processor modules used in the Cisco 7505 router

Note Interface processors designed for the CxBus will work with the CyBus in the Cisco 7505; however, they will not be able to utilize the increased bandwidth capability provided by the CyBus.

- EIP—Ethernet Interface Processor
- FEIP—Fast Ethernet Interface Processor.
- FIP—FDDI Interface Processor

- FRU—A field-replaceable unit is a system component that must be replaced by a Cisco-certified service provider
- FSIP—Fast Serial Interface Processor
- HIP— HSSI Interface Processor
- MIP—MultiChannel Interface Processor
- OIR—Online insertion and removal feature that allows you to replace interface processors without interrupting system power
- RSP1—Route Switch Processor
- Spare—a system component that can be replaced by someone other than a Cisco-certified service provider
- TRIP—Token Ring Interface Processor

Physical Description

The Cisco 7505 uses the RSP1 and up to four interface processors. Figure 1-1 shows the interface processor end of the chassis.

The interface processor end of the router comprises the five processor slots and power supply. The power supply bay contains the power supply, which has an AC-input receptacle (or a DC-input terminal block), the power switch, and a power status indicator. (See Figure 1-1; the configuration shown is arbitrary.)

The processor slots contain the RSP1 and up to four interface processors. When viewing the router from the interface processor end, the RSP1 is in the top slot (the RSP slot or slot 4). The remaining four slots are numbered from the bottom up beginning with slot 0 (the bottom slot) through slot 3 (the second slot from the top).

The four interface processor slots support any combination of network interface types: Ethernet, Token Ring, serial, and so forth. The RSP1 and interface processors are keyed with guides on the backplane to prevent them from being fully inserted in the wrong slot.

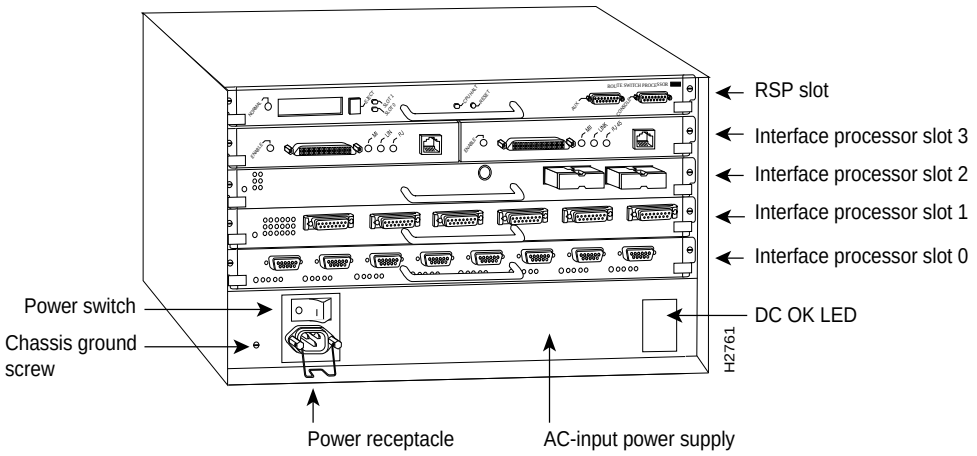
The interface processors all have the same key and can be placed in slots 0 through 3 only. The RSP1 has a unique key and can be placed in slot 4 only.

The RSP1 and interface processors (collectively referred to as *processor modules* in this description) slide into the processor slots in the rear of the router and connect directly to the backplane; there are no internal cables to connect. Spring-loaded ejector levers help to ensure that a processor module is either fully connected to the backplane or fully disconnected from it.

Captive installation screws, one at each end of the interface processor faceplate, also ensure proper seating in the slot and prevent the processor module from disengaging from the backplane connectors. (During operation, the system will hang if the connection between the processor module connector and any of the backplane pins is interrupted.) Empty slots contain a blank interface processor filler (the metal interface processor carrier without a board, LEDs, or connectors) to maintain proper airflow through the chassis.

Note Do not stack the router with any other equipment or place it directly on a floor. For clearance requirements and rack-mount installation considerations, refer to the section “Site Environment” in the chapter “Preparing for Installation.”

Figure 1-1 Cisco 7505 Router, Interface Processor View—AC-Input Power Supply Shown

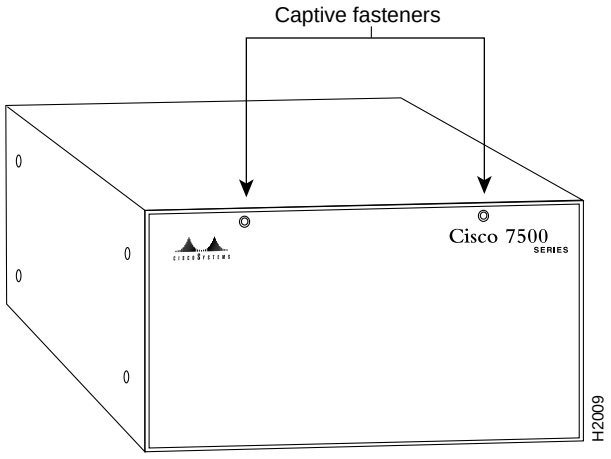


On the back of the router, LEDs on the RSP1 and power supply indicate status. The normal LED lights to indicate that the system is in a normal operating state.

For descriptions of internal environmental thresholds and status levels, refer to the section "Environmental Monitoring and Reporting Functions" in this chapter.

The front, or noninterface processor end, of the Cisco 7505 has a removable panel that is secured with two captive slotted fasteners. (See Figure 1-2.) Removing the panel provides access to the internal components: the power supply and fan tray.

Figure 1-2 Router Chassis Cover Panel



One 600-watt (W), AC-input power supply or one 600W, DC-input power supply is standard equipment in the Cisco 7505.

The Cisco 7505 operates as either a tabletop or rack-mounted unit. A rack-mount kit is standard equipment that is included with all Cisco 7505 chassis. The kit provides the hardware needed to mount the router in a standard 19-inch equipment rack, or in a variety of other equipment rack configurations. When the router is not mounted in a rack, place it on a table or on a sturdy platform. Do not stack the router with any other equipment or place it on the floor.

Chassis Specifications

Table 1-1 lists the Cisco 7505 physical specifications and power requirements.

Table 1-1 Cisco 7505 System Specifications

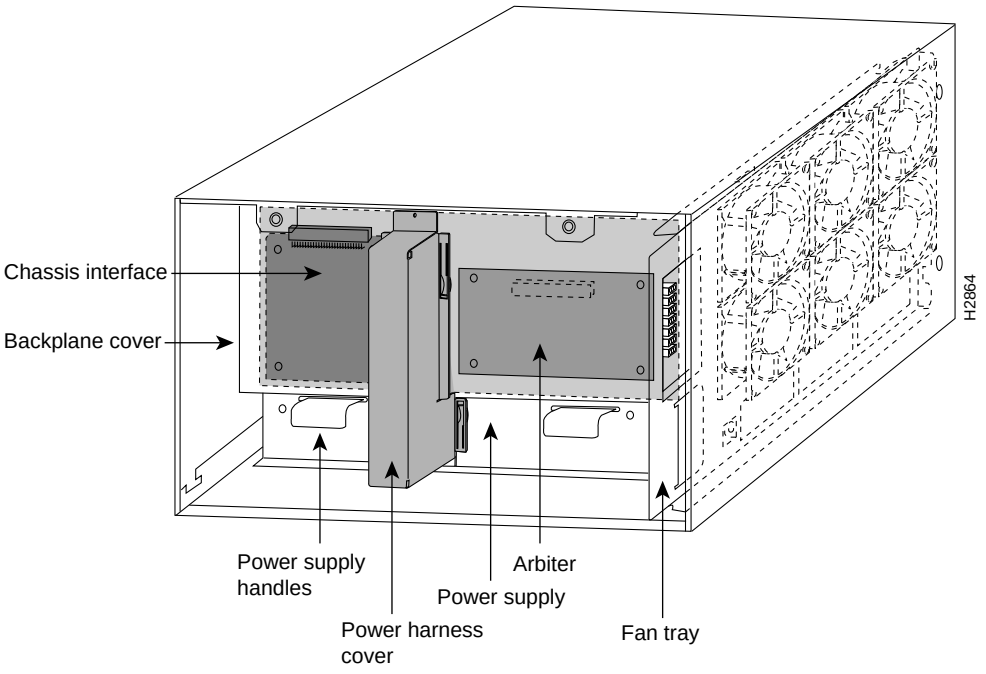
Description	Specification
High-speed backplane	5-slot, 1.067-Gbps CyBus: 4 interface processor slots plus the RSP slot
Dimensions (H x W x D)	10.5 x 17.5 x 17.0" (26.67 x 44.45 x 43.18 cm) Chassis depth including power cord and cable management fixture is 19" (48.26 cm)
Weight	Chassis only (including power supply and fan array): 46 lb (20.87 kg) Chassis fully configured with RSP1 and 4 interface processors: 70 lb (31.75 kg)
Power dissipation	600W maximum configuration with AC-input power supply 600W maximum configuration with DC-input power supply 540W typical with maximum configuration
Heat dissipation	715W (2440 Btus/hr)
AC-input voltage	100 to 240 volts AC (VAC), wide input with power factor corrector (PFC)
Frequency	50 to 60 Hz
AC-input current	9A maximum @ 100 VAC 4A maximum @ 240 VAC at 600W
DC-input voltage	–40 volts DC (VDC) minimum in North America (–56 VDC in the Europe Community) –48 VDC nominal in North America (–60 VDC in the Europe Community) –52 VDC maximum in North America (–72 VDC in the Europe Community) 20A maximum at –48 VDC and 16A maximum @ –60 VDC
DC voltages supplied and maximum, steady-state current ratings for AC- and DC-input	+5.2 VDC @ 75 amps (A) +12 VDC @ 15A –12 VDC @ 3A +24 VDC @ 5A
DC-input cable	10 AWG (American Wire Gauge); recommended minimum wire gauge
DC-input hold-up time	10 milliseconds (ms) of output after the DC input has been interrupted
Airflow	Side-to-side through chassis by variable-speed, 6-fan array
Operating temperature	32 to 104 F (0 to 40 C)
Nonoperating temperature	–4 to 149 F (–20 to 65 C)
Relative humidity	10 to 90%, noncondensing
Software requirement	Cisco Internetwork Operating System (Cisco IOS) Release 10.3 (3) or later
Regulatory compliance approvals	Safety: UL 1950, CSA 22.2-No. 950, EN60950, EN41003, AUSTEL TS001, AS/NZS 3260, and IEC 801-2, 3, 4, 5, and 6 EMI: FCC Class A, VCCI Class II, and CISPR 22 B (EN 55022) Conducted Emissions

Note For a chassis footprint, additional dimensions, and clearance requirements for the router perimeter, refer to the section “Site Requirements” in the chapter “Preparing for Installation.”

Internal Components

The main internal components in the Cisco 7505 are the arbiter, chassis interface, power supply, fan tray, and backplane, all of which are located in the noninterface processor end of the router. (See Figure 1-3.) Only the power supply and fan tray are replacable, and are available as spares.The power supply, which sits on the interior chassis floor, operates on AC input (or DC input for the DC-input supply) and provides DC voltages to the system components. The six individual fans on the fan tray move cooling air through the chassis interior to prevent components from overheating. The backplane contains the data buses for information exchange and distributes power throughout the system. The following sections describe the spares and other major system components.

Figure 1-3 Internal Components at Noninterface Processor End of Router



Arbiter

The arbiter, which arbitrates traffic on the CyBus and generates the CyBus clock, is a printed circuit board that is mounted to the front (noninterface processor side) of the system backplane. (See Figure 1-3 for its relative location—the arbiter is *not* a spare.) The arbiter controls traffic across the CyBus by prioritizing access requests from interface processors to ensure that each request is processed and to prevent any interface processor from jeopardizing the CyBus and interfering with the ability of the other interface processors to access the RSP1. The arbiter provides the following services for the system:

- CyBus clock generation—Generates the 16.667-megahertz (MHz) clock and provides a private copy of the clock to the RSP1 and each interface processor.
- CyBus arbitration—Arbitrates interface processor requests to transmit commands on the CyBus. The arbitration is based on a round-robin priority scheme to ensure that all interface processors have access to a known portion of the CyBus bandwidth.
- Global lock arbitration—Arbitrates interface processor and RSP1 requests for the global lock, a synchronization primitive used to control RSP1 and interface processor access to shared data structures.

Power Supply

The Cisco 7505 comes equipped with one 600W, AC-input power supply (shown in Figure 1-4) or one 600W, DC-input power supply. The AC-input power supply operates on AC-input power and supplies DC power to the internal components. The DC-input power supply operates on DC-input power and supplies DC power to the internal components. Table 1-1, earlier in this chapter, lists the acceptable AC-input and DC-input ranges and the internal operating DC voltages that are supplied.

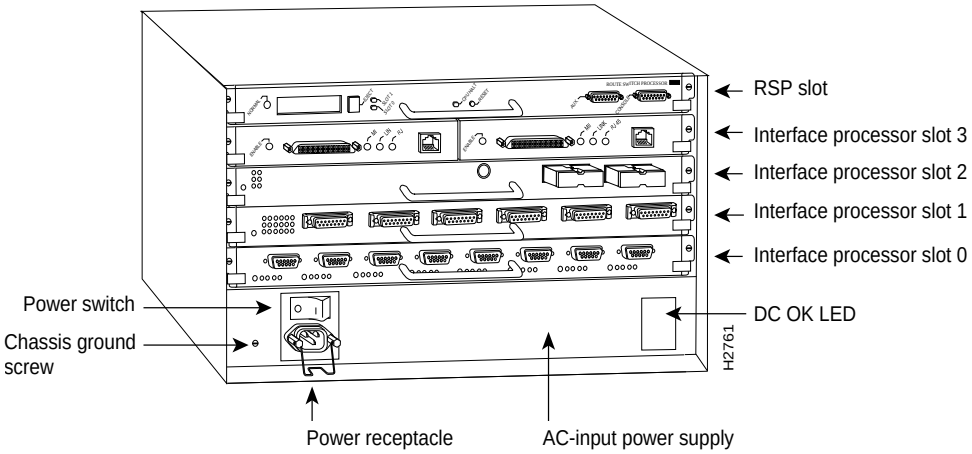
At the noninterface processor end of the router, two handles on the power supply provide grip points for pulling the power supply out of the chassis. (See Figure 1-3.) Two Phillips-head screws secure the power supply to the chassis interior. The power supply delivers DC power to the internal components through a wiring harness that plugs into a polarized receptacle to the noninterface processor side of the backplane. An aluminum cover shields the harness and power connection. The backplane distributes the DC voltages to the fan tray, arbiter, chassis interface, and interface processor bus connectors.

The AC power receptacle (or DC-input terminal block), power on/off switch (or circuit breaker-type switch on the DC-input power supply), and status LED are on the interface processor end of the power supply. (See Figure 1-4.) A modular power cable connects the AC-input power supply to the site AC power source. A cable retention clip on the power supply AC receptacle prevents the cable from being pulled out accidentally.

The DC-input is supplied by a three-lead, 10-AWG cable that you provide. Cable strain relief is in the form of a nylon cable tie that you provide.

On the AC-input and DC-input power supplies, the power switch turns the power supply on and starts the system. To the left of the power switch and receptacle is a chassis ground screw that provides a chassis ground connection for ESD equipment or a grounding wire.

Figure 1-4 Cisco 7505, Interface Processor End—AC-Input Power Supply Shown



On the AC-input and DC-input power supplies, the green DC OK LED indicates the status of the power supply and internal DC voltages. The DC OK LED stays on when all of the following conditions are met:

- AC-input power supply is on and receiving 100 to 240 VAC, 50 to 60 Hz source power

OR

- DC-input power supply is on and receiving –48 VDC in North America (or –60V in the European Community)
- Either the AC-input or DC-input power supply is providing the +5, +12, –12, and +24 VDC to internal components
- All internal DC voltages are within tolerance

If the AC or DC source power or any of the internal DC voltages exceeds allowable tolerances, the DC OK LED goes off and the system environmental monitor messages indicate the line that is out of tolerance. Because the RSP1 (which uses +5, +12, –12 VDC), and the fan tray (which uses +24 VDC) are both required for operation, the system will probably shut down if any internal voltages reach an out-of-tolerance state.

Inside the AC-input or DC-input power supply, two small fans draw cooling air through the power supply interior. The air flows in one side of the supply and out the other side, following the same direction as the chassis cooling air. (See Figure 1-5.)

In addition to the environmental monitoring performed by the system, the power supply monitors its own temperature and internal voltages. If the supply detects an overvoltage, or overtemperature condition, it shuts down to avoid damage to the power supply or other system components. For a description of power-supply shutdown conditions and thresholds, refer to the section "Environmental Monitoring and Reporting Functions" in this chapter.

The AC-input and DC-input power supplies are available as spares for immediate onsite replacement if the existing power supply fails. The chapter "Maintaining the Router" provides power supply replacement instructions. In addition, detailed, up-to-date instructions are included with all spares when they are shipped from the factory.

Chassis Interface

The chassis interface provides the environmental monitoring (ENVM) and power supply monitoring functions for the Cisco 7505. (See Figure 1-3 for its relative location—the chassis interface is *not* a spare.) The chassis interface isolates the CPU and system software from chassis-specific variations. The chassis interface attaches directly to the system backplane.

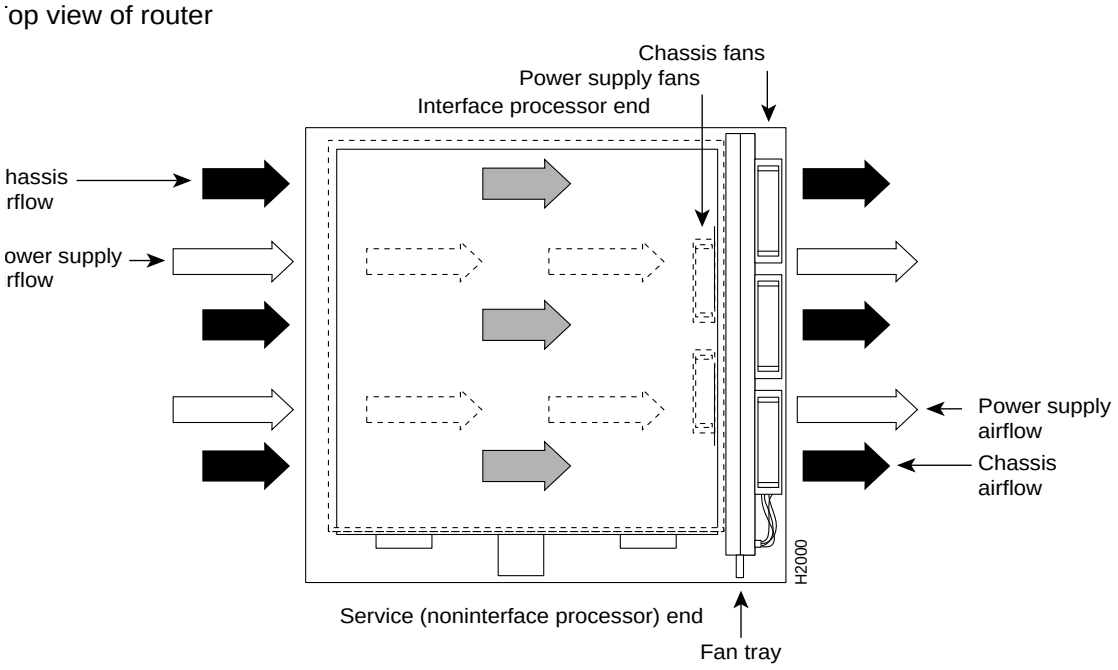
The functions of the chassis interface are as follows:

- Report backplane type
- Report arbiter type
- Monitor power supply status
- Monitor fan/blower status
- Monitor temperature sensors on the RSP1
- Provide router power up/down control
- Provide power supply power-down control

Fan Tray

An array of six individual axial fans draw cooling air through the chassis interior to maintain an acceptable operating temperature for the internal components. The *fan tray* comprises the six fans and a printed circuit board (with the control circuits) mounted on a metal plate. (See Figure 1-5.) The fan tray slides into the right side of the chassis from the noninterface processor end of the router. (See Figure 1-3.) The fans draw air in through the inlet vents on the opposite side of the chassis, across the processor modules and other internal components, and out through the exhaust vents adjacent to the fan tray. Figure 1-5 shows the airflow path. The sides of the chassis must remain unobstructed to ensure adequate airflow and prevent overheating inside the chassis. (See the section "Site Requirements" in the chapter "Preparing for Installation.")

Figure 1-5 Internal Airflow—Top-Down View



A fan control board on the fan tray monitors and controls the operation of the variable-speed fans. The variable-speed feature enables quieter operation by allowing the fans to operate at less than maximum speed when doing so provides adequate cooling air to maintain an acceptable operating temperature inside the chassis.

A temperature sensor on the fan array monitors the exhaust air temperature. When the exhaust air temperature is within the normal operating range, the fans operate at the slowest speed, which is 55 percent of the maximum speed. If the temperature inside the chassis exceeds the normal range, the fan control board increases the fan speed to provide additional cooling air to the internal components. If the temperature continues to rise, the fan control board linearly increases the fan speed until the fans reach full speed (100 percent). If the internal temperature exceeds the specified threshold, the system environmental monitor shuts down all internal power to prevent equipment damage from excessive heat.

All six fans in the array must be operational. If the system detects a failed or failing fan, it will display a warning message on the console screen. If the condition is not corrected within two minutes, the entire system will shut down to avoid an overtemperature condition and shutdown.

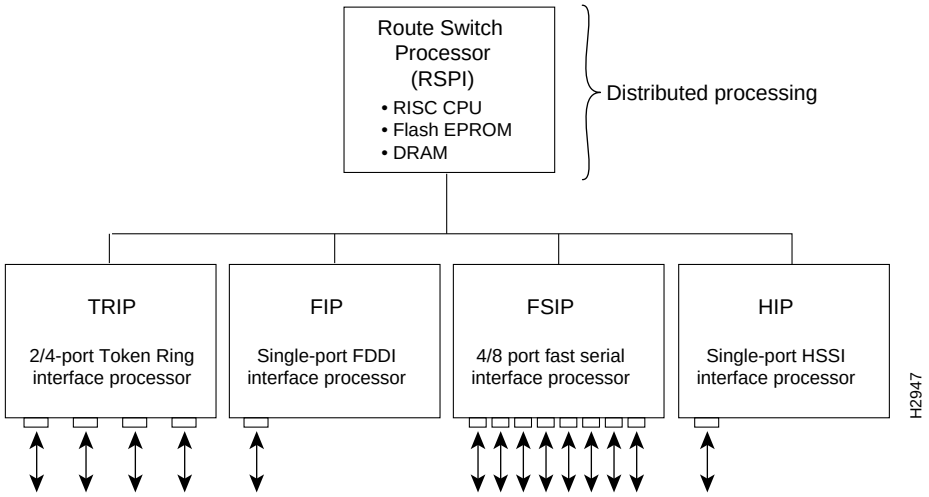
For specific thresholds and message descriptions, refer to the section "Environmental Monitoring and Reporting Functions," in this chapter, and to the section "Troubleshooting the Cooling Subsystem," in the chapter "Troubleshooting the Installation."

Note The fan tray is available as a spare; however, individual fans are not replaceable. If a single fan fails, you *must* replace the fan tray. The chapter "Maintaining the Router" provides fan tray replacement instructions.

System Backplane

The CyBus backplane transfers information at 1.067 Gbps. Figure 1-6 shows the basic system architecture. The RSP1 provides distributed processing and control for the interface processors, and controls communication between high-speed interface processors (interface processor-to-interface processor) and the system processor (interface processor-to-system processor).

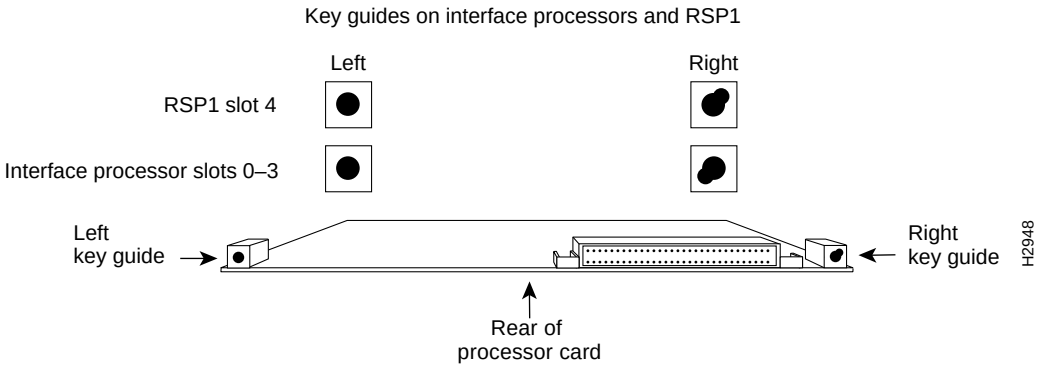
Figure 1-6 Example of Router System Architecture—Not All Processors Represented



The backplane slots are keyed so that the processor modules can be installed only in the slots designated for them. Keys on the backplane fit into two key guides on each module. (See Figure 1-7.) Although the RSP1 uses unique keys, all four interface processor slots use the same key, so you can install an interface processor in any interface processor slot, but not in the RSP slot.

Caution When installing an RSP1 or interface processor, ensure that you are installing it in the appropriate slot to avoid damaging the key guides or the backplane.

Figure 1-7 Backplane Slot Keys



Route Switch Processor

The RSP1, shown in Figure 1-8, is the main system processor in the router. The RSP1 contains the system CPU, the system software (in Flash memory), the system memory components, and it maintains and executes the management functions that control the system.

The RSP1 contains the following components:

- Orion/R4600 Reduced Instruction Set Computing (RISC) processor, used for the central processing unit (CPU). The CPU runs at an external clock speed of 50 megahertz (MHz) and an internal clock speed of 100 MHz.
- Bank of hardware (MAC-layer) addresses for the interface ports
- Most of the memory components used by the system, including onboard Flash memory
- Air-temperature sensors for environmental monitoring

In addition to the preceding system components, the RSP1 contains and executes the following management functions that control the system:

- Sending and receiving routing protocol updates
- Managing tables and caches
- Monitoring interface and environmental status
- Providing Simple Network Management Protocol (SNMP) management and the console/Telnet interface

The RSP1 *must* be installed in the top slot, which is labeled *Slot 4* on the backplane and *RSP* to the left of the slots. (See Figure 1-9.) The high-speed switching section of the RSP1 communicates with and controls the interface processors on the high-speed CyBus. This section decides the destination of a packet and switches it based on that decision. The single enabled LED (on the front of the chassis) lights to indicate that the RSP1 is enabled for operation.

Memory Components

Figure 1-8 shows the locations of the various types of memory on the RSP1, and Table 1-2 lists the functions of each.

Figure 1-8 Route Switch Processor

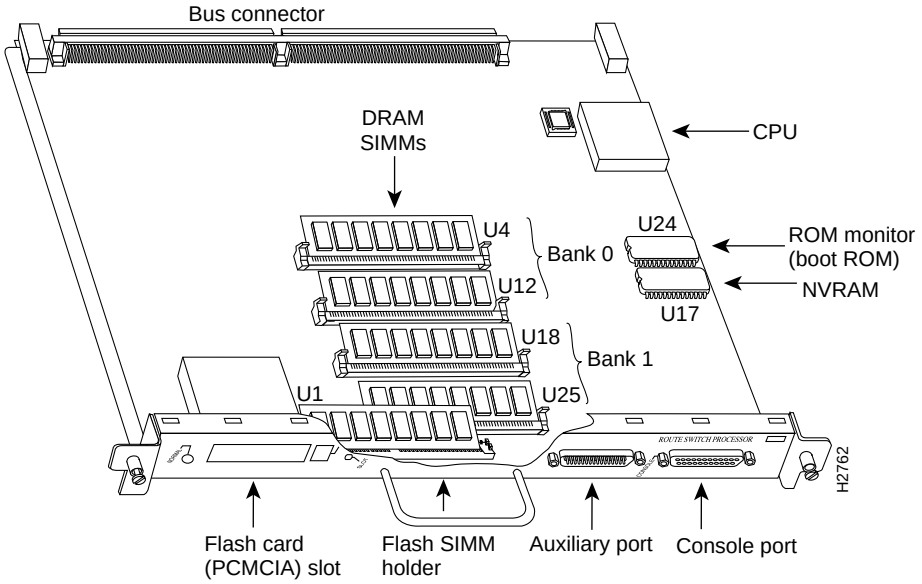


Table 1-2 RSP1 Memory Components

Type	Size	Quantity	Description	Location
DRAM[1]	16 to 128 MB[2]	2 to 4	8, 16, or 32-MB SIMMs (depending on maximum DRAM required).	Bank 0: U4 and U12 Bank 1: U18 and U25
NVRAM[3]	128 KB[4]	1	Nonvolatile EPROM[5] for the system configuration file.[6]	U17
Flash SIMM[7] Flash Card	8 MB 16 MB	1 Up to 2	Contains the Cisco IOS images on the RSP1. Contains the Cisco IOS images on up to two PCMCIA[8] cards.	U1 Slot 0, Slot 1
Boot ROM[9]	256 KB	1	EPROM for the ROM monitor program.	U24

1. Dynamic random-access memory.
2. MB = megabyte.
3. NVRAM = nonvolatile random-access memory.
4. KB = kilobyte.
5. EPROM = erasable programmable read-only memory.
6. A system configuration file is contained in NVRAM, which allows the software to control several system variables.
7. SIMM = single inline memory module.
8. PCMCIA = Personal Computer Memory Card International Association.
9. ROM = read-only memory.

System Software

The Cisco 7505 router supports downloadable system software and microcode for most upgrades, which enables you to remotely download, store, and boot from a new image. The publication *Upgrading Software and Microcode in Cisco 7XXX Series Routers* (Document Number 78-1144-xx), which accompanies all upgrade kits, provides instructions for upgrading from floppy disk or Flash memory card.

Flash memory on the RSP1 contains the default system software. An EPROM device on each interface processor contains the latest interface processor microcode version, in compressed form. At system startup, an internal system utility scans for compatibility problems between the installed interface processor types and the bundled microcode images, then decompresses the images into running memory (DRAM). The bundled microcode images then function the same as images loaded from the microcode EPROM.

DRAM

DRAM stores routing tables, protocols, and network accounting applications. The standard RSP1 configuration is 16 MB of DRAM, with up to 128 MB available through SIMM upgrades.

Note When upgrading DRAM, you must use SIMMs from an approved vendor. To ensure that you obtain the most current vendor information, obtain the list from Cisco Information Online (CIO) or the Technical Assistance Center (TAC). Refer to the "Service and Support" card in your warranty package.

NVRAM

The nonvolatile random-access memory (NVRAM) stores the system configuration and the environmental monitoring logs, and is backed up with built-in lithium batteries that retain the contents for a minimum of five years. When replacing an RSP1, back up your configuration to a remote server so that you can retrieve it later. (See the Timesaver note that follows.)

Timesaver Before replacing an RSP1, back up the running configuration to a Trivial File Transfer Protocol (TFTP) file server so that you can later retrieve it. If the configuration is not saved, the entire configuration will be lost—inside the NVRAM on the removed RSP1—and you will have to reenter it manually. This procedure is not necessary if you are temporarily removing an RSP1 you will reinstall; lithium batteries retain the configuration in memory until you replace the RSP1 in the system.

Flash Memory

Either the imbedded (onboard) Flash memory (on a SIMM) or the Flash memory on a PCMCIA card, allows you to remotely load and store multiple Cisco Internetwork Operating System Cisco (Cisco IOS) software and microcode images and backup configurations.

You can download a new image over the network or from a local server and then add the new image to Flash memory or replace the existing files. You can then boot routers either manually or automatically from any of the stored images. Flash memory also functions as a TFTP server to allow other servers to remotely boot from stored images or to copy them into their own Flash memory.

EEPROM

An electrically erasable programmable read-only memory (EEPROM) component on the RSP1 (and each interface processor) stores board-specific information such as the board serial number, part number, controller type, hardware revision, and other details unique to each board.

Note This EEPROM is not a spare and cannot be programmed in the field.

Jumpers

Because the RSP1 uses a software configuration register for system configuration and Flash memory for system software images, there are no user-configurable jumpers on the RSP1.

LEDs

The two LEDs on the RSP1 indicate the system and RSP1 status. The normal LED is on when the system is operational, and during normal operation and the CPU halt LED should be off. The CPU halt LED, which goes on only if the system detects a processor hardware failure, should never be on. For complete descriptions of the LED states, refer to the appendix “Reading LED Indicators.”

Serial Ports

Two asynchronous EIA/TIA-232 serial ports on the RSP1, the console and auxiliary ports, provide the means for connecting a terminal, modem, or other device for configuring and managing the system. A data circuit-terminating equipment (DCE) EIA/TIA-232 receptacle console port on the RSP1 provides a direct connection for a console terminal.

Note EIA/TIA-232 was known as recommended standard RS-232 before its acceptance as a standard by the Electronic Industries Association (EIA) and Telecommunications Industry Association (TIA).

The adjacent data terminal equipment (DTE) EIA/TIA-232 plug auxiliary port supports flow control and is often used to connect a modem, a channel service unit (CSU), or other optional equipment for Telnet management of the attached device.

The console and auxiliary ports support asynchronous transmission. Asynchronous transmission uses control bits to indicate the beginning and end of characters, rather than precise timing. The serial interface ports on the FSIP support synchronous transmission, which maintains precise clocking between the transmitter and receiver by sending frames of information that comprise separate clock signals along with the data signals. When connecting serial devices, ensure that the devices support the proper transmission timing methods for the respective port: asynchronous for the console and auxiliary ports, and synchronous for the FSIP serial ports.

Interface Processors

An interface processor comprises a modular, self-contained interface board and one or more network interface connectors in a single 11 x 14-inch unit. All interface processors support OIR, so you can install and remove them without opening the chassis and without turning off the chassis power. (The early serial interface processor, known as the SX-SIP or PRE-FSIP, will not operate in the Cisco 7505; see the following Caution.)

The RSP1, which is a required system component, always resides in slot 4. (See Figure 1-9.)

The remaining four slots (0 through 3, from the bottom to the top) are available for any combination of the following interface processors:

- AIP—For interface types and specifications, refer to the chapter "Preparing for Installation," in the section "ATM Connection Equipment" or to the section "ATM Interface Processor" in this chapter.
- CIP—For any combination of one or two bus and tag and/or one or two Enterprise System Connection (ESCON) interfaces.

Note For specific bus and tag and ESCON interface configurations and specifications, refer to the chapter "Preparing for Installation" in the section "Channel Attachment Connection Equipment," or to the section "Channel Interface Processor" in this chapter.

- EIP—For two, four, or six attachment unit interface (AUI) ports, each of which operates at up to 10 Mbps
- FEIP—For up to two 100BASE-T, RJ-45 or Media Independent Interface (MII) ports. The interfaces on an FEIP can both be configured at 100 Mbps, half duplex (HDX) or full duplex (FDX), for a maximum aggregate bandwidth of 200 Mbps.
- TRIP—For two or four high-speed (4 or 16 Mbps) Token Ring, DB-9 ports.
- FIP—For one high-speed (100 Mbps), single attachment or dual attachment port (PHY A/PHY B) in any combination of single-mode and multimode ports (such as single-single, multi-single, and so forth)
- FSIP— For either four or eight fast (up to 8 Mbps, or 16 Mbps aggregate with 8 ports), synchronous serial ports, including EIA-530, EIA/TIA-232, EIA/TIA-449, E1-G.703/G.704, V.35, and X.21 interfaces
- HIP—For a single HSSI port, which can be clocked up to 52 Mbps.
- MIP—For up to two channelized T1 interfaces that operate at T1 speed—up to 1.544 Mbps, or up to two channelized E1 interfaces that operate at E1 speed—up to 2.048 Mbps

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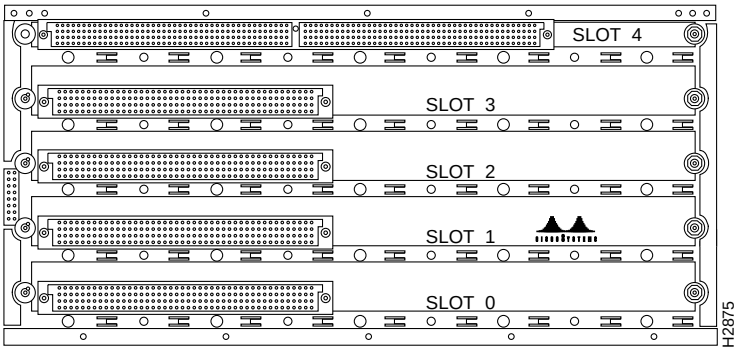
Note T1 and E1 interfaces cannot be mixed on a single MIP.

Caution The early serial interface processor (SX-SIP or PRE-FSIP) cannot be used in the Cisco 7505 (the SX-SIP requires SxBus connectors that are not present in the Cisco 7505). To prevent system problems, do not use SX-SIP or PRE-FSIP cards in the Cisco 7505.

Figure 1-9 Slot Numbering in the Cisco 7505 Card Cage



The microcode on each interface processor contains board-specific software instructions. New features and enhancements to the system or interfaces are often implemented in microcode upgrades. The Cisco 7505 supports downloadable microcode for most maintenance upgrades, which enables you to download new microcode images remotely and store them in Flash memory. You can then use software commands to instruct the system to load a specific microcode image from Flash memory or to load the default microcode image from ROM.

System software upgrades also can contain upgraded microcode images, which will load automatically when the new software image is loaded.

Note The software and interface processor microcode images are carefully optimized and bundled to work together. Overriding the bundle can result in incompatibility between the various interface processors in the system.

Caution To ensure proper operation of the system and to avoid system problems, you should use *only* the microcode images that are bundled with system software.

Each interface processor has a unique bank of status LEDs, and all have a common enabled LED at the left end of the interface processor faceplate. The enabled LED goes on when the RSP1 has completed initialization of the interface processor for operation, indicating that, as a minimum, the interface processor is correctly connected to the backplane, that it is receiving power, and that it contains a valid microcode version. If any of these conditions is not met, or if the initialization fails for other reasons, the enabled LED stays off. Additional LEDs on each interface processor type indicate the state of the interfaces.

The appendix “Reading LED Indicators,” describes the specific LED states of each.

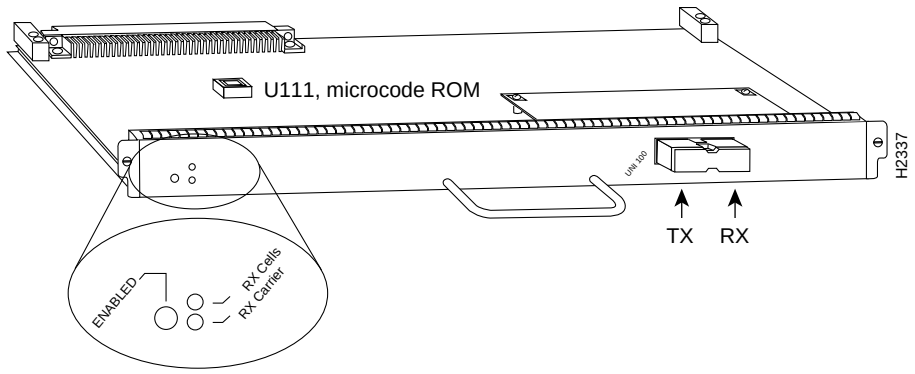
The following sections describe each interface processor type.

ATM Interface Processor

The AIP provides a direct connection between the high-speed CyBus and the external networks. (See Figure 1-10.) The AIP can support the following data transmission rates: transparent asynchronous transmitter/receiver interface (TAXI) 4B/5B at 100 Mbps, Synchronous Optical Network/Synchronous Digital Hierarchy (SONET/SDH) at 155 Mbps, E3 at 34 Mbps, and DS3 at 44.736 Mbps.

The default AIP microcode resides on an EPROM in socket U111.

Figure 1-10 AIP—Shown with the 100 Mbps, User-to-Network Interface (UNI) PLIM



The specific physical layer interface module (PLIM) on the AIP determines the type of ATM connection. A maximum of four AIP modules are supported on the Cisco 7505. There are no restrictions on slot locations or sequence; an AIP can be installed in any available interface processor slot.

The AIP supports the following features:

- Multiple rate queues.
- Reassembly of up to 512 buffers simultaneously. Each buffer represents a packet.
- Support for up to 2,048 virtual circuits.
- Support for both ATM Adaptation Layer (AAL) 5 and AAL3/4.
- Exception queue, which is used for event reporting. Events such as CRC errors are reported to the exception queue.
- Raw queue, which is used for all raw traffic over the ATM network. Raw traffic includes operation and maintenance (OAM) cells and Interim Local Management Interface (ILMI) cells. (ATM signaling cells are not considered raw.)

For more information on the AIP, refer to the sections “Distance Limitations and Interface Specifications” and “ATM Connection Equipment” in the chapter “Preparing for Installation.” Also refer to the *Asynchronous Transfer Mode Interface Processor (AIP) Installation and Configuration* publication (Document Number 78-1214-xx), which is available on UniverCD or in print.

Channel Interface Processor

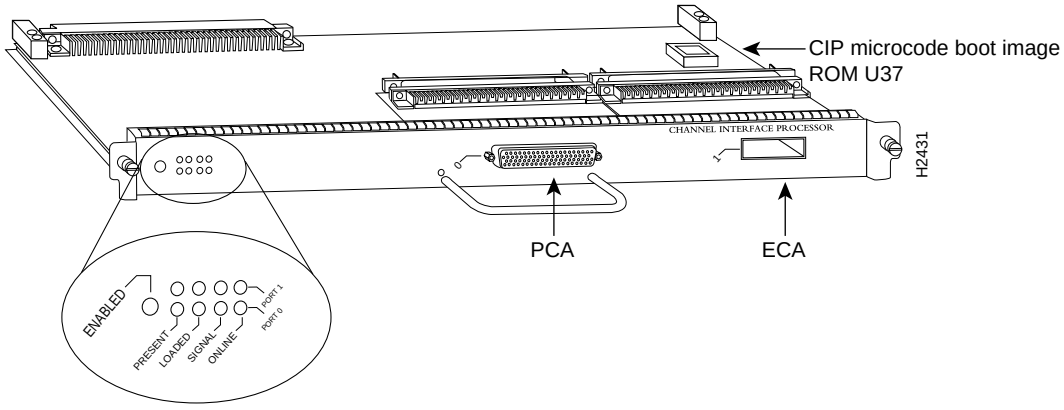
The CIP provides up to two channel-attached interfaces, eliminating the need for a separate front-end processor. (See Figure 1-11.) Although a maximum of four CIPs can be used in the Cisco 7505, three CIPs is the recommended maximum, so that the fourth slot can provide a wide-area network (WAN) connection, such as the FSIP. The CIP interfaces are combinations of a bus and tag (also called an original equipment manufacturer's interface [OEMI] and a parallel I/O interface) adapter and/or an Enterprise Systems Connection (ESCON) adapter. The bus and tag adapter is called the Parallel Channel Adapter (PCA) and the ESCON adapter is called the ESCON Channel Adapter (ECA). The PCA and ECA connect directly to the CIP, and any combination of the two adapters can be used.

Note The ECA and PCA adapters can be upgraded or replaced in the field by a Cisco certified maintenance provider *only.*

The supported processor input/output architectures for the CIP include ESA/390 for ESCON and System/370, 370/Xa, and ESA/390 for bus and tag. The ESCON interface is capable of a data rate up to 17 megabytes per second (MBps) and the bus and tag interface is capable of a data rate up to 4.5 MBps.

Only the CIP microcode boot image resides on an EPROM in socket U37. (See Figure 1-11.) The entire CIP microcode image is located in the software/microcode bundle.

Figure 1-11 Channel Interface Processor



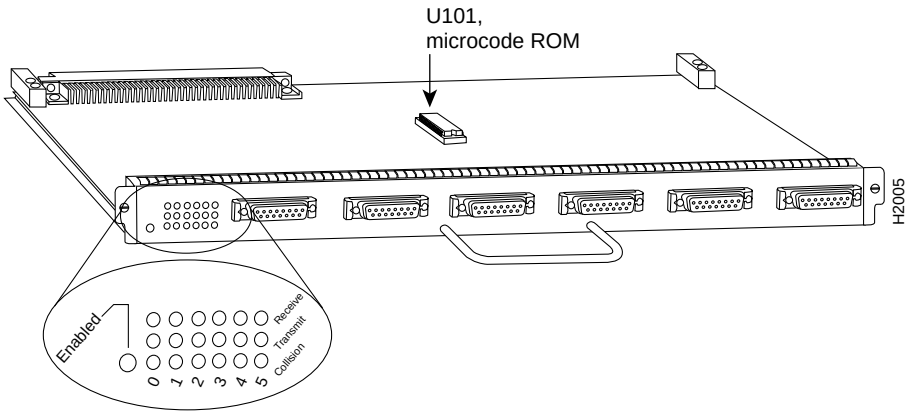
For more information on the CIP, refer to the *Channel Interface Processor (CIP) Installation and Configuration* publication (Document Number 78-1342-xx), which is available on UniverCD or in print.

Ethernet Interface Processor

The EIP, shown in Figure 1-12, provides two, four, or six Ethernet ports that operate at up to 10 Mbps. Each port supports both Ethernet Version 1 and IEEE 802.3/Ethernet Version 2 interfaces. A bit-slice processor provides a high-speed data path between the EIP and other interface processors.

The default EIP microcode resides on an EPROM in socket U101.

Figure 1-12 Ethernet Interface Processor



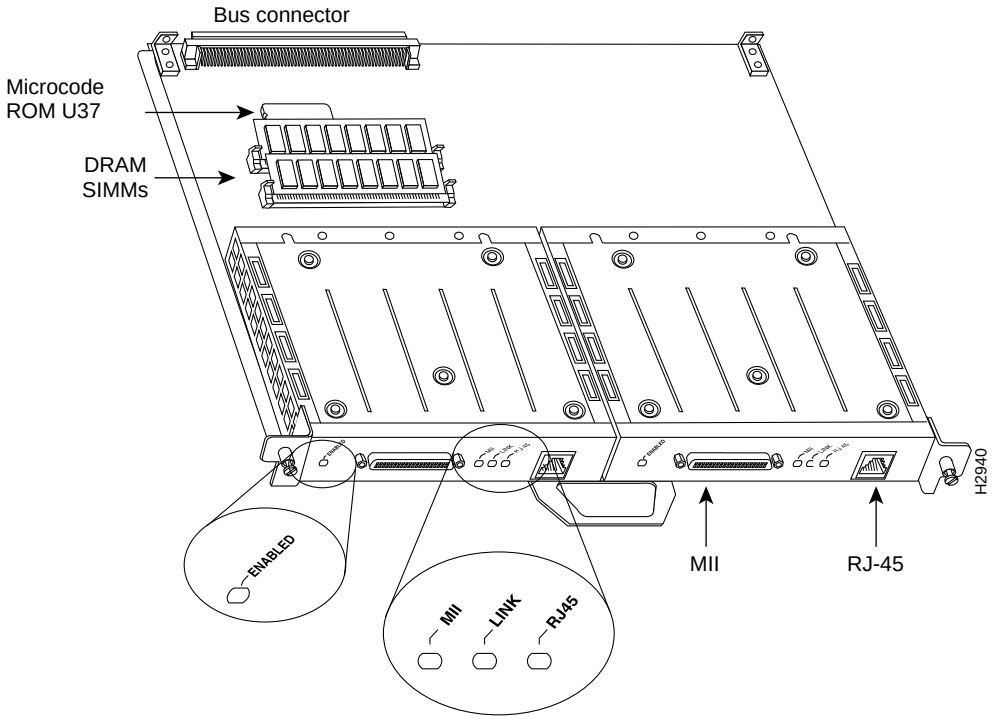
The EIP is available with two, four, or six ports. The Cisco 7505 supports a maximum of four EIPs for a maximum of 24 Ethernet ports. Each port requires an Ethernet transceiver or a media attachment unit (MAU) and attachment unit interface (AUI) cable to connect to the external network. For descriptions of Ethernet transceivers and AUIs, refer to the section “Ethernet Connection Equipment,” in the chapter “Preparing for Installation.” For descriptions of Ethernet network connections, refer to the section “Ethernet Connections” in the chapter “Installing the Router.”

Each port on the EIP automatically supports both Ethernet Version 1 and Version 2/IEEE 802.3 connections. When an interface is connected to an EIP port, the port automatically adjusts to the interface type. The ports are independent, so you can mix both versions on one EIP.

Fast Ethernet Interface Processor

The FEIP provides up to two 100-Mbps, IEEE 802.3u 100BASE-T ports. (Figure 1-13 shows a two-port FEIP.) IEEE 802.3u specifies several different physical layers for 100BASE-T: 100BASE-TX—100BASE-T half duplex, over Category 5, unshielded twisted-pair (UTP), EIA/TIA-568-compliant cable; 100BASE-FX—100BASE-T full duplex, over twisted pair or optical fiber); and 100BASE-T4—100BASE-T full duplex, using Category 3 and 4 cabling with four pairs (also called *4T+)*.

Figure 1-13 Fast Ethernet Interface Processor



Following are the product numbers associated with the FEIP:

- CX-FEIP-1TX= (interface processor with one 100BASE-TX port adapter)
- CX–FEIP-2TX= ((interface processor with two 100BASE-TX port adapters)

The interfaces on an FEIP can both be configured at 100 Mbps, half duplex (HDX) or full duplex (FDX), for a maximum aggregate bandwidth of 200 Mbps. The FEIP microcode boot image resides in an EPROM in socket location U37.

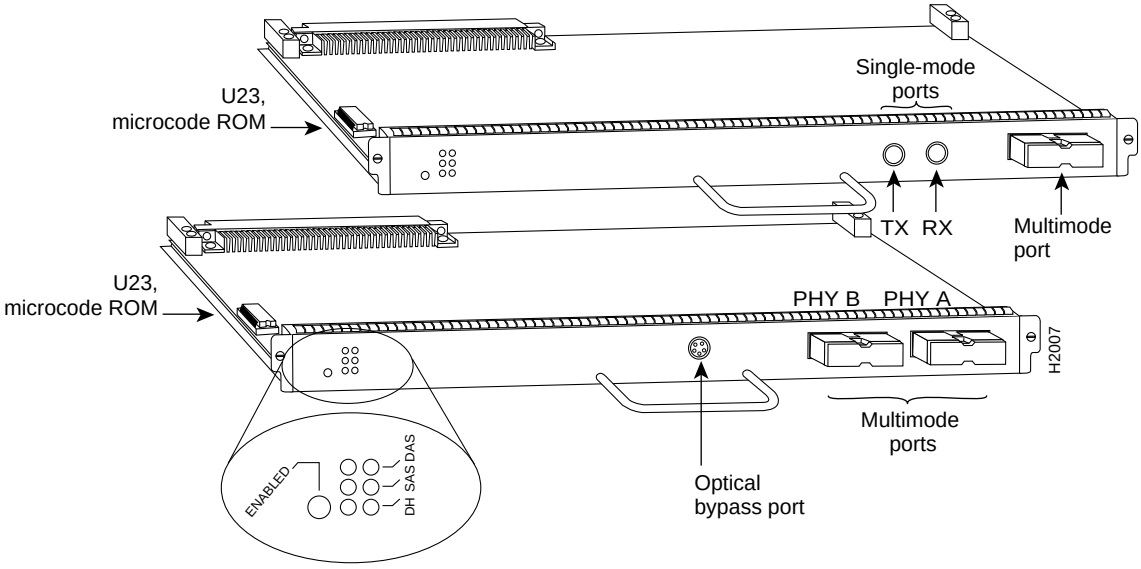
Fiber Distributed Data Interface Processor

The FIP contains the industry-standard AMD SuperNet chipset for interoperability, and a 16-million instructions per second (mips) processor for high-speed (100 Mbps) interface rates. The Cisco 7505 supports a maximum of four FIPs for a total of four FDDI interfaces. There are no restrictions on slot locations or sequence; you can install a FIP in any available interface processor slot.

Figure 1-14 shows a multimode/multimode FIP on the bottom and a single-mode/multimode FIP on the top. The FIP supports single attachment stations (SASs), dual attachment stations (DASs), dual homing, and optical bypass for both multimode and single-mode operation. The FIP complies with ANSI X3.1 and ISO 9314 FDDI standards.

The default FIP microcode resides on an EPROM in socket U23.

Figure 1-14 FDDI Interface Processor



Each FIP provides a single network interface for both multimode and single-mode FDDI networks. The two FIP connectors are available in any combination of multimode (MIC) or single-mode (FC) connectors for matching multimode and single-mode fiber in the same FDDI network. The following combinations are available:

- CX-FIP-MM—FDDI PHY-A multimode, PHY-B multimode interface processor, with an optical bypass switch mini-DIN connector
- CX-FIP-MS—FDDI PHY-A multimode, PHY-B single-mode interface processor
- CX-FIP-SM—FDDI PHY-A single-mode, PHY-B multimode interface processor
- CX-FIP-SS—FDDI PHY-A single-mode, PHY-B single-mode interface processor, with an optical bypass switch mini-DIN connector

Each FIP provides the interface for connection to a Class A, DAS (with primary and secondary rings), or to a Class B, SAS (with only a primary ring). The multimode MIC or single-mode FC ports on the FIP provide a direct connection to the external FDDI network.

A six-pin mini-DIN connector on the multimode/multimode and single-mode/single-mode FIPs provides the connection for an optical bypass switch. When the interface is shut down, the bypass switch allows the light signal to pass directly from the receive port to the transmit port on the bypass switch, completely *bypassing* the FIP transceivers. The bypass switch does not repeat the signal, and significant signal loss may occur when transmitting to stations at maximum distances. Optical bypass switches typically use a six-pin DIN or mini-DIN connector. A DIN-to-mini-DIN adapter cable (CAB-FMDD) is included with the FIP to allow connection to either type of connector. For a detailed description of optical bypass and FDDI connections, refer to the section "FDDI Connection Equipment," in the chapter "Product Overview." For descriptions of FDDI network connections, refer to the section "FDDI Connections," in the chapter "Installing the Router."

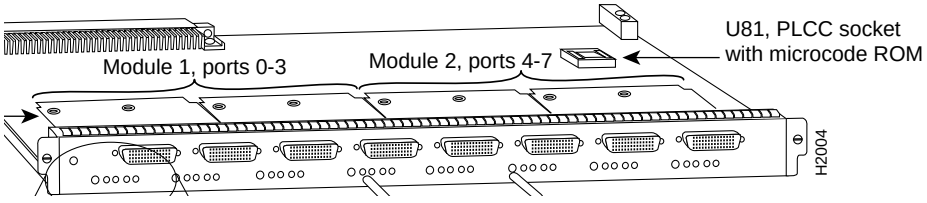
Fast Serial Interface Processor

The FSIP provides four or eight channel-independent, synchronous serial ports that support full duplex operation at T1 (1.544 Mbps) and E1 (2.048 Mbps) speeds. Each port supports any of the available interface types: EIA/TIA-232, EIA/TIA-449, V.35, X.21, EIA-530, and E1-G.703/G.704.

Figure 1-15 shows an eight-port FSIP. The eight ports are divided into two four-port modules, each of which is controlled by a dedicated Motorola MC68040 processor and contains 128 kilobytes (KB) of static random-access memory (SRAM). Each module can support up to 4 T1 or 4 E1 interfaces, and an aggregate bandwidth of up to 16 Mbps at full duplex operation. The type of electrical interface, the amount of traffic, and the types of external data service units (DSUs) connected to the ports affect actual rates. For information on setting up high-speed interfaces, refer to the section "Configuring the FSIP," in the chapter "Maintaining the Router."

The default FSIP microcode resides on a PLCC-type EPROM in socket U81.

Figure 1-15 Fast Serial Interface Processor



Each FSIP comprises an FSIP board with two or four port adapters installed.

Note Additional port adapters are available as spares so that you can replace one that fails; however, *you cannot upgrade a four-port FSIP to an eight-port by adding port adapters*.

The 4-port FSIP is not constructed to support additional ports after it leaves the factory. It contains the circuitry to control only one 4-port module. For port adapter descriptions, refer to the section "Universal Serial Port Adapters" in this chapter.

The Cisco 7505 supports up to four FSIPs for a maximum of 32 high-speed serial interfaces. There are no restrictions on slot locations or sequence; you can install FSIPs in any available interface processor slots. For descriptions of serial connection equipment, refer to the section "Serial Connection Equipment," in the chapter "Product Overview." For examples of network connections, refer to the section "Serial Connections" in the chapter "Product Overview."

All interface types except EIA-530 and E1-G.703/G.704 are individually configurable for operation with either external timing (DTE mode) or internal timing (DCE mode); EIA-530 operates with external timing only. In addition, all interfaces support nonreturn to zero (NRZ) and nonreturn to zero inverted (NRZI) format, and both 16-bit and 32-bit cyclic redundancy checks (CRCs). The default configuration is for NRZ format and 16-bit CRC. You can change these default settings with software commands. (See the section "Configuring the FSIP" in the chapter "Maintaining the Router.")

In order to provide a high density of ports, the FSIP uses special *port adapters* and *adapter cables*. A port adapter is a daughter card that provides the physical interface for two FSIP ports. Both ports use the same high-density, 60-pin universal receptacle that supports all interface types. The adapter cable connected to the port determines the interface type and mode.

The interface ports are not set to a default mode or for a default clock source, so there are no software commands required to enable internal or external timing (DCE or DTE). Each port automatically supports the mode of the port adapter cable when one is connected. However, there is no default clock rate set. You must set the clock rate on all DCE ports with the **clockrate** command before the port can operate with an external timing signal. To use the port as a DCE interface, you must set the clock rate and connect a DCE adapter cable. To use the port as a DTE interface, you need only connect a DTE adapter cable to the port. If you connect a DTE cable to a port on which a clock rate is set, the system will ignore the clock rate until a DCE cable is attached. For example, you can change an interface from an EIA/TIA-232 to a V.35 by replacing the adapter cable, or change the mode of an EIA/TIA-232 DTE port by replacing the EIA/TIA-232 DTE cable with an EIA/TIA-232 DCE cable, provided that you have already specified a clock rate for the port.

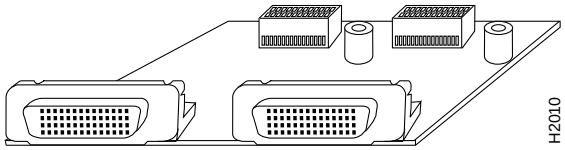
Note Although no software configuration is necessary to enable internal clocking for DCE mode, you cannot bring up a DCE interface until you set the clock rate. For a brief description of the **clockrate** command, refer to the section "Configuring the FSIP" in the chapter "Maintaining the Router." For complete command descriptions and instructions, refer to the related software command reference publication.

Universal Serial Port Adapters

The FSIP uses special universal serial port adapters and adapter cables to allow the high density (eight) of interface ports on an FSIP, regardless of the size or form factor of the connectors typically used with each electrical interface type. Figure 1-16 shows a universal port adapter with the 60-pin connectors that support all interface types. The adapter cable connected to the port determines the interface type and mode.

The universal port adapters are replaceable daughter cards mounted to the FSIP, and each provides two high-density connectors for two FSIP ports. (See Figure 1-16.) The 60-pin D-shell receptacle supports EIA/TIA-232, V.35, EIA/TIA-449, X.21, and EIA-530.

Figure 1-16 Universal Serial Port Adapter



Universal

The router (FSIP) end of all universal-type adapter cables is a 60-pin plug that connects to the 60-pin port (receptacle) on the FSIP. The network end of the cable is an industry-standard connector for the type of electrical interface that the cable supports: DB-25 for EIA/TIA-232 and EIA-530, DB-37 for EIA/TIA-449, DB-15 for X.21, or a standard V.35 block connector. For most interface types, the adapter cable for DTE mode uses a plug at the network end, and the cable for DCE mode uses a receptacle at the network end. However, V.35 adapter cables are available with either a V.35 plug or a receptacle for either mode, and EIA-530 is available only in DTE mode with a DB-25 plug. Factory-installed 4-40 thumbscrews are standard at the network end of all cable types except V.35. A metric conversion kit with M3 thumbscrews is included with each cable to allow connection to devices that use metric hardware.

The FSIP is shipped from the factory with two or four dual-port adapters installed. Additional port adapters are available as spares so that you can replace one that fails; however, *you cannot upgrade a four-port FSIP to an eight-port by adding port adapters*. The four-port FSIP is manufactured with only one four-port module and processor.

For port adapter replacement instructions, refer to the section “Removing and Replacing Serial Port Adapters” in the chapter “Maintaining the Router.”

Note The appendix “Cabling Specifications” provides adapter cable pinouts. However, because the FSIP uses a special high-density port that requires special adapter cables for each electrical interface type, we recommend that you obtain serial interface cables from the factory.

E1-G.703/G.704 Port Adapter

The FSIP E1-G.703/G.704 port adapter (see Figure 1-17) connects the Cisco 7505 with 2-Mbps leased-line services. The interface eliminates the need for a separate, external data termination unit to convert a standard serial interface (such as V.35) to a G.703/G.704/G.732 interface.

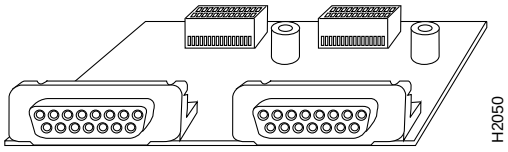
The FSIP can be configured to support up to eight E1-G.703/G.704 ports (four ports per module, two modules per FSIP). FSIP bandwidth can be allocated by the user and the maximum aggregate bandwidth per four-port module is 16 Mbps, full duplex. We recommend that you leave one port on each module shut down to avoid exceeding this 16-Mbps maximum per module. Each of the four interfaces can operate up to 2.048 Mbps, which potentially presents a load greater than 16 Mbps, full duplex, if all four interfaces are configured. Eight E1-G.703/G.704 ports can be supported up to the 16-Mbps aggregate bandwidth capability; however, it is not possible to simultaneously support eight E1-G703/G.704 ports at 100-percent peak bandwidth utilization, without exceeding the 16-Mbps maximum per module.

Two versions of the E1-G.703/G.704 interface are available: one supports balanced mode, and the other supports unbalanced mode. Neither the modes nor the cables are interchangeable; you cannot configure a balanced port to support an unbalanced line, nor can you attach an interface cable intended for a balanced port to an unbalanced port.

The FSIP E1-G.703/G.704 interface supports both framed and unframed modes of operation, a loopback test, and a four-bit CRC. The interface can operate with either a line-recovered or an internal clock signal. The FSIP is configured at the factory with from one to four E1-G.703/G.704 port adapters. Each port adapter provides two 15-pin D-shell (DB-15) receptacles, which support only E1-G.703/G.704 interfaces.

Note The FSIP E1-G.703/G.704 interface uses a DB-15 receptacle for both the balanced and unbalanced ports. The label adjacent to the port indicates whether the port is balanced or unbalanced; you must connect the correct type of interface cable for the port to operate.

Figure 1-17 FSIP E1-G.703/G.704 Port Adapter



E1-G.703/G.704

The FSIP end of all E1-G.703/G.704 adapter cables is a DB-15 connector. At the network end, the adapter cable for unbalanced connections uses a BNC connector. The adapter cables for balanced mode are available with several connector types to accommodate connection standards in different countries. You must use the proprietary cables to connect the E1-G.703/G.704 port to your network.

Cables for balanced and unbalanced mode are available with the following types of network-end connectors:

- Balanced (120-ohm) twinax split at the network end, with separate transmit and receive cables, each with a BNC connector
- Balanced (120-ohm) cable with a DB-15 connector at the network end
- Unbalanced (75-ohm) coaxial cable with BNC connectors at the network end (used primarily for connection in the United Kingdom)

In addition, some connections require bare-wire connections (directly to terminal posts).

Table 1-3 lists the model numbers and descriptions of the E1-G.703/G.704 port adapters and cables.

Table 1-3 Model Numbers and Descriptions of E1-G.703/G.704 Port Adapter and Cables

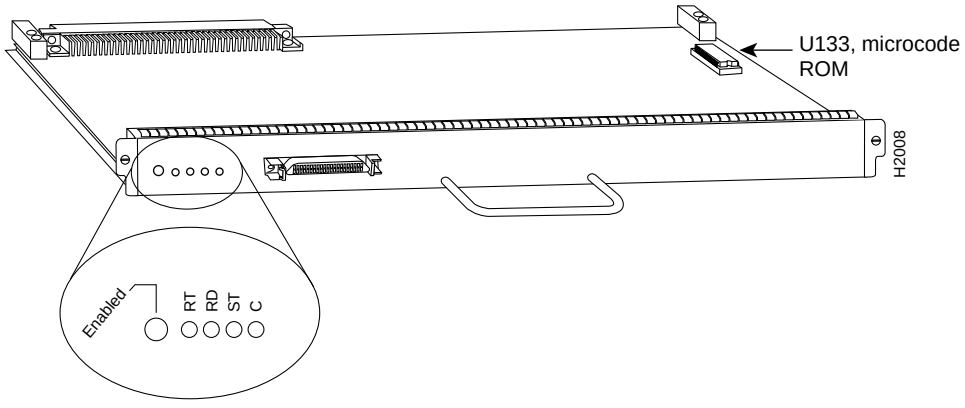
Port Adapter and Cable Model Numbers	Description
PA-7KF-E1/120=[1]	Dual-port E1-G.703/G.704 120 ohm, balanced
PA-7KF-E1/75=	Dual-port E1-G.703/G.704 75 ohm, unbalanced
CAB-E1-TWINAX=	E1 cable twinax 120 ohm, balanced, 5 m
CAB-E1-DB15=	E1 cable, DB-15, 120 ohm, balanced, 5 m
CAB-E1-BNC=	E1 cable BNC 75 ohm, unbalanced, 5 m

1. The appended equal sign (=) indicates a spare part.

HSSI Interface Processor

The HIP, shown in Figure 1-18, provides a full-duplex, synchronous serial interface for transmitting and receiving data at rates of up to 52 Mbps. HSSI, recently standardized as EIA/TIA 612/613, provides access to services at T3 (45 Mbps), E3 (34 Mbps), and SONET STS-1 (51.82 Mbps) rates. The actual rate of the interface depends on the external DSU and the type of service to which it is connected. The default HIP microcode resides on an EPROM in socket U133.

Figure 1-18 HSSI Interface Processor



The HIP interface port is a 50-pin, SCSI-II-*type* receptacle. You need a HSSI interface cable to connect the HIP with an external DSU.

Note Although the HSSI port and cable are physically similar to SCSI-II format, the HSSI specification is more stringent than that for SCSI-II, and we cannot guarantee reliable operation if a SCSI-II cable is used.

A null modem cable allows you to connect two collocated routers back to back to verify the operation of the HSSI interface or to build a larger node by linking the routers directly. For a description of HSSI network and null modem connections, refer to the section "HSSI Connections," in the chapter "Installing the Router." The appendix "Cabling Specifications" provides connector pinouts and cable assembly drawings. The Cisco 7505 supports up to four HIPs for a total of four interfaces. There are no restrictions on slot locations or sequence; you can install a HIP in any available interface processor slot.

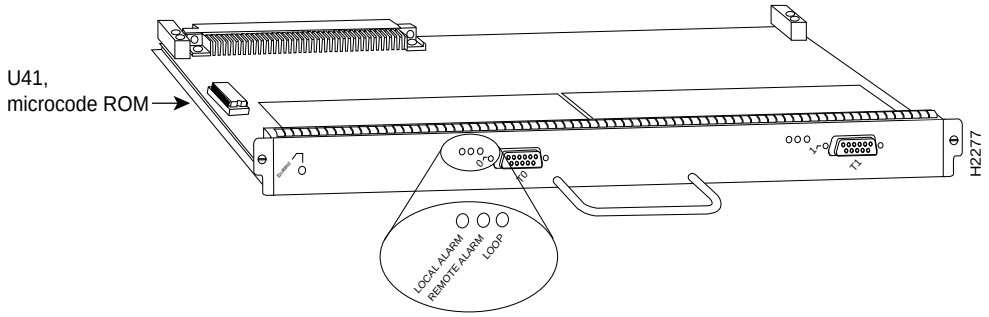
MultiChannel Interface Processor

The MIP provides up to two channelized T1 or up to two channelized E1 connections via serial cables to a CSU. On the MIP, two controllers can each provide up to 24 T1 channel-groups or 30 E1 channel-groups. Each channel-group is presented to the system as a serial interface that can be configured individually. The Cisco 7505 supports a maximum of four MIPs for a total of 8 MIP ports and up to 240 serial interfaces. There are no restrictions on slot locations or sequence; you can install a MIP in any available interface processor slot.

The MIP, shown in Figure 1-19, provides one or two controllers for transmitting and receiving data bidirectionally at the T1 rate of 1.544 Mbps or one or two controllers for transmitting and receiving data bidirectionally at the E1 rate of 2.048 Mbps. For wide-area networking, the MIP can function as a concentrator for a remote site. The MIP supports OIR, which allows you to remove and install a MIP while the system is operating, without shutting down system power.

The default MIP microcode resides on an EPROM in socket U41.

Figure 1-19 MultiChannel Interface Processor—Dual-Port Module Shown



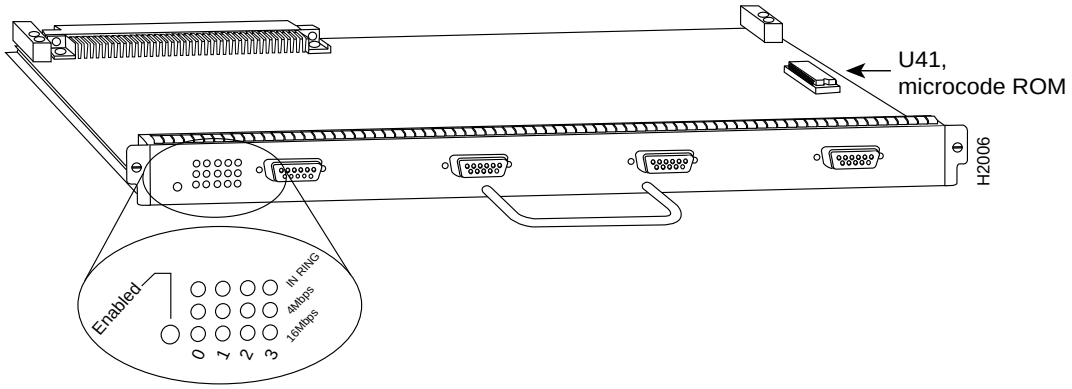
Note The MultiChannel Interface Processor (MIP) and the Channel Interface Processor (CIP) use entirely dissimilar interfaces and have entirely dissimilar functions within the router.

Token Ring Interface Processor

The TRIP, shown in Figure 1-20, provides two or four Token Ring ports for interconnection with IEEE-802.5 and IBM Token Ring media. The TRIP uses the IBM 16/4-Mbps chipset with an imbedded, performance-enhanced interface driver and a 16.7-MHz bit-slice processor for high-speed processing. The speed on each port is independently software-configurable for either 4 or 16 Mbps.

The default TRIP microcode resides on an EPROM in socket U41.

Figure 1-20 Token Ring Interface Processor



The TRIP is available with two or four ports. The Cisco 7505 supports up to four TRIPs for a maximum of 16 Token Ring ports. Each port requires a media access unit (MAU) to connect the DB-9 TRIP connectors to the external Token Ring networks. There are no restrictions on slot locations or sequence; you can install a TRIP in any available interface processor slot.

For descriptions of Token Ring connectors and MAUs, refer to the section “Token Ring Connection Equipment,” in the chapter “Preparing for Installation.” For descriptions of Token Ring network connections, refer to the section “Token Ring Connections,” in the chapter “Product Overview.”

Functional Overview

This section describes functions that support the router's high availability and maintainability. The OIR feature enables you to quickly install new interfaces without interrupting system power or shutting down existing interfaces. The environmental monitoring and reporting functions continuously monitor temperature and voltage points in the system, and provide reports and warning messages that enable you to quickly locate and resolve problems and maintain uninterrupted operation. These descriptions will help you become familiar with the capabilities of the router and the functional differences between the Cisco 7505 and other products.

Port Densities

The four available interface slots support any combination of network interface processors, or any four of the same type for the following maximum port densities:

- Up to 24 Ethernet interfaces
- Up to 8 channel attachment interfaces
- Up to 16 Token Ring interfaces
- Up to 4 FDDI interfaces
- Up to 32 serial interfaces
- Up to 4 HSSI interfaces
- Up to 240 multichannel serial interfaces
- Up to 4 ATM interfaces

You can install any combination of interface processors in any of the three available interface processor slots.

Note Although there are no restrictions on either the number of interfaces possible or their location with respect to the RSP1, you might want to keep one interface processor slot open for a wide-area network (WAN) or local-area network (LAN) interface depending on your configuration.

Addresses and Port Numbers

Each interface (port) in a Cisco 7505 uses different types of addressing. The *slot/port number* is the actual physical location of the interface connector (port) within the chassis (slot). The system software uses the slot/port numbers to control activity within the router and to display status information. These slot/port numbers are not used by other devices in the network; they are specific to the individual router and its internal components and software.

The *Media Access Control (MAC)-layer* or *hardware* address is a standardized data link layer address that is required for every port or device that connects to a network. The Cisco 7505 uses a specific method to assign and control the MAC-layer addresses of its interfaces.

The following sections describe how the Cisco 7505 assigns and controls both the slot/port numbers and MAC–layer addresses for interfaces within the chassis.

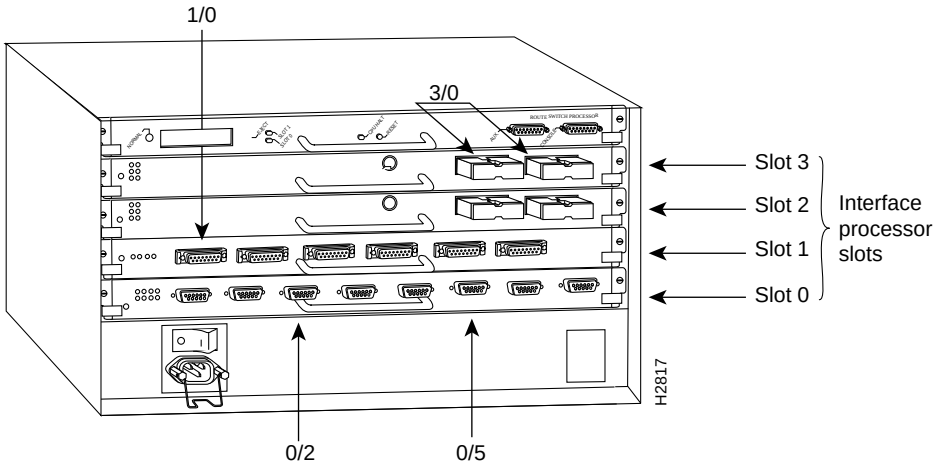
Slot/Port Numbers

In the Cisco 7505, slot/port numbers specify the actual location of each interface port on the router interface processors. (See Figure 1-21.) The number uses the format *slot*/*port*. The first number identifies the slot in which the interface processor is installed (0 through 3, beginning at the bottom slot). The second number identifies the port number on the interface processor. The ports on each interface processor are numbered sequentially from *left* to *right* beginning with the port 0.

Interface ports maintain the same slot/port number regardless of whether other interface processors are installed or removed. However, when you move an interface processor to a different slot, the first number changes to reflect the new slot number. For example, on a six-port EIP in slot 1, the slot/port number of the first port (on the left) is 1/0 and that of the right-most port is 1/5. If you remove the EIP from slot 1 and install it in slot 2, the slot/port numbers of those same ports become 2/0 and 2/5, respectively.

Figure 1-21 shows some of the port numbers of a sample system.

Figure 1-21 Interface Port Address Examples



Interface slots are numbered 0 to 3 from the bottom slot up. The port numbers always begin at 0 and are numbered from left to right. The number of additional ports (/1, /2, and /3) depends on the number of ports available on an interface. For example, FDDI interfaces are always /0, because each FIP supports one interface. (The multiple connectors on the FIP can be misleading, but they provide multiple attachment options for a *single* FDDI interface.) Ethernet interfaces can be numbered from /0 through /5 because EIPs support up to six Ethernet ports. Serial interfaces on an eight-port FSIP are numbered /0 through /7, and so forth.

You can identify interface ports by physically checking the slot/port number on the back of the router or by using software commands to display information about a specific interface or all interfaces in the router. To display information about every interface, use the **show interface** command without arguments. To display information about a specific interface, use the **show interface** command with the interface type and slot/port number in the format **show interface** [*type slot/port*]. If you abbreviate the command (**sho int**) and do not include arguments, the system interprets the command as **show interface** and displays the status of all interfaces.

Following is an example of how the **show interface** command, used without arguments, displays status information (including the physical slot/port number) for each interface in the router. In the following example, most of the status information for each interface is omitted.

```
Router# sho int

Serial0/0 is up, line protocol is up
  Hardware is cxBus Serial
  Internet address is 131.108.123.4, subnet mask is 255.255.255.0
  (display text omitted)
Ethernet1/2 is up, line protocol is up
  Hardware is cxBus Ethernet, address is 0000.0c02.d0f1 (bia 0000.0c02.d0f1)
  (display text omitted)
Fddi2/0 is administratively down, line protocol is down
  Hardware is cxBus Fddi, address is 0000.0c02.adc2 (bia 0000.0c02.adc2)
  Internet address is 131.108.31.4, subnet mask is 255.255.255.0
  (display text omitted)
```

You can also use arguments such as the interface type (**ethernet**, **tokenring**, **fddi**, **serial**, **hssi**, and so forth) and the port address (slot/port) to display information about a specific interface only.

The following example shows the display for the first (far left) Ethernet port on an EIP in slot 1:

```
Router# show int ether 1/0

Ethernet1/0 is up, line protocol is up
  Hardware is cxBus Ethernet, address is 0000.0c02.d0ce (bia 0000.0c02.d0ce)
  Internet address is 131.108.31.7, subnet mask is 255.255.255.0
  MTU 1500 bytes, BW 10000 Kbit, DLY 1000 usec, rely 255/255, load 1/255
  Encapsulation ARPA, loopback not set, keepalive set (10 sec)
  (display text omitted)
```

For complete command descriptions and instructions, refer to the related software configuration and command reference documentation.

MAC-Layer Address Allocator

All network interface connections (ports), except serial ports, require a unique MAC layer address, which is also known as a *hardware* address. Typically, the MAC address of an interface is stored on a memory component that resides directly on the interface circuitry; however, the OIR feature requires a different method.

The OIR feature allows you to remove an interface processor and replace it with another identically-configured one. If the new interfaces match the interfaces you removed, the system immediately brings them on line. In order to allow OIR, an address allocator with unique MAC addresses is stored in a memory device on the backplane. Each address is reserved for a specific slot/port in the router regardless of whether an interface resides in that port. The MAC addresses are assigned to the ports in sequence; the first address is assigned to the first port on the interface processor in slot 0 and the last address is assigned to the last port on the interface processor in slot 3. This address scheme allows you to remove interface processors and insert them into other routers without causing the MAC addresses to move around the network or be assigned to multiple devices.

Note that if the MAC addresses were stored on each interface processor, OIR would not function because you could never replace one interface with an identical one; the MAC addresses would always be different. Also, each time an interface was replaced, other devices on the network would have to update their data structures with the new address, and, if they did not do so quickly enough, could cause the same MAC address to appear in more than one device at the same time.

Storing the MAC addresses in a memory device on the backplane avoids these problems. When an interface is replaced with another identical interface, there is no need for other devices in the network to update their data structures and routing tables.

Note Storing the MAC addresses for every port in one central location means they stay with the memory device on which they are stored.

Online Insertion and Removal—An Overview

The OIR feature allows you to install and replace interface processors while the system is operating; you do not need to notify the software or shut down the system power. All interface processors (AIP, CIP, EIP, FEIP, FIP, FSIP, HIP, MIP, and TRIP) support OIR. The following is a functional description of OIR for background information only; for specific procedures for installing and replacing interface processors on line, refer to the section "Installing and Configuring Processor Modules" in the chapter "Maintaining the Router."

Caution All interface processors support OIR; however, *you must shut down the system before removing or installing the RSP1*, which is a required system component. Removing an RSP1 while the system is operating will cause the system to shut down, and might damage memory files.

Each RSP1 and interface processor contains a bus connector with which it connects to the system backplane. The bus connector is a set of tiered pins, in three lengths. The pins send specific signals to the system as they make contact with the backplane. The system assesses the signals it receives and the order in which it receives them to determine what event is occurring and what task it needs to perform, such as reinitializing new interfaces or shutting down removed ones.

For example, when you insert an interface processor, the longest pins make contact with the backplane first, and the shortest pins make contact last. The system recognizes the signals and the sequence in which it receives them. The system expects to receive signals from the individual pins in this logical sequence, and the ejector levers help to ensure that the pins mate in this sequence. When you remove or insert an interface processor, the backplane pins send signals to notify the system, which then performs as follows:

1. Rapidly scans the backplane for configuration changes and does not reset any interfaces.
2. Initializes all newly inserted interface processors, noting any removed interfaces and placing them in the administratively shutdown state.
3. Brings all previously configured interfaces on the interface processor back to the state they were in when they were removed. Any newly inserted interfaces are put in the administratively shutdown state, as if they were present (but unconfigured) at boot time. If a similar interface processor type has been reinserted into a slot, then its ports are configured and brought on line up to the port count of the original interface processor.

OIR functionality enables you to add, remove, or replace interface processors with the system online, which provides a method that is seamless to end users on the network, maintains all routing information, and ensures session preservation.

When you insert a new interface processor, the system runs a diagnostic test on the new interfaces and compares them to the existing configuration.

If this initial diagnostic test fails, the system remains off line for another 15 seconds while it performs a second set of diagnostic tests to determine whether or not the interface processor is faulty and if normal system operation is possible.

If the second diagnostic test passes, which indicates that the system is operating normally and the new interface processor is faulty, the system resumes normal operation but leaves the new interfaces disabled.

If the second diagnostic test fails, the system crashes, which usually indicates that the new interface processor has created a problem in the bus and should be removed. The system brings on line only interfaces that match the current configuration and were previously configured as up; all other interfaces require that you configure them with the **configure** command. On interface processors with multiple interfaces, only the interfaces that have already been configured are brought on line.

For example, if you replace a single-PCA CIP with a dual-PCA CIP, only the previously configured interface is brought on line automatically; the new PCA interface remains in the administratively shutdown state until you configure it and bring it on line.

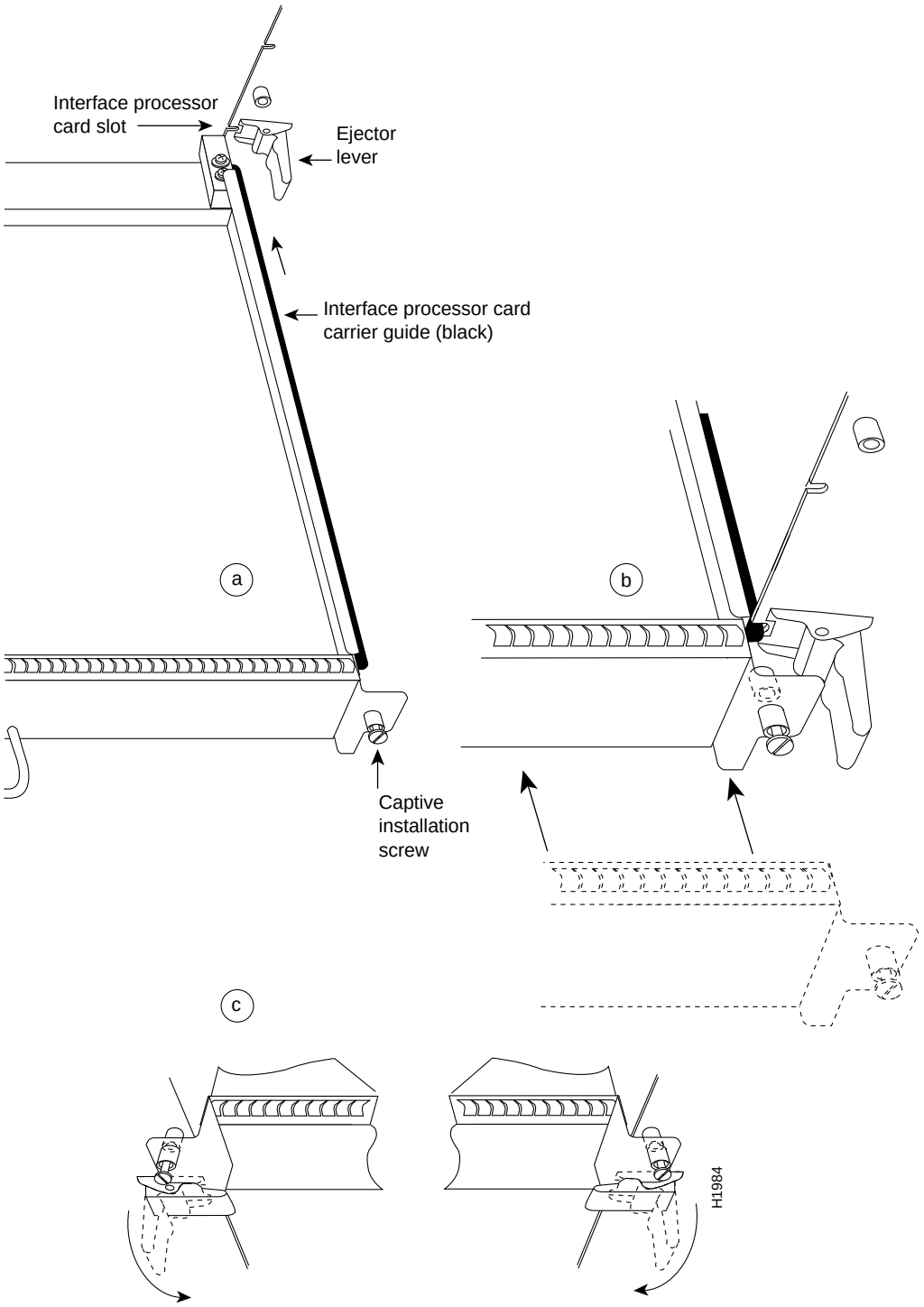
Caution When removing or replacing interface processors, you can avoid erroneous failure messages by allowing at least 15 seconds for the system to reinitialize before removing or inserting another interface processor.

The function of the ejector levers (see Figure 1-22) is to align and seat the interface processor bus connectors in the backplane. Failure to use the ejector levers and insert the interface processor properly can disrupt the order in which the pins make contact with the backplane. Following are examples of incorrect insertion practices and results:

- Using the handle to force an interface processor all the way into the slot can pop the ejectors out of their springs. If you then try to use the ejectors to seat the interface processor, the first layer of pins (which are already mated to the backplane) can disconnect and then remate with the backplane, which the system interprets as a board failure.
- Using the handle to force or slam an interface processor all the way into the slot can also damage the pins on the board connectors if they are not aligned properly with the backplane.
- When using the handle (rather than the ejectors) to seat an interface processor in the backplane, you may need to pull the interface processor back out and push it in again to align it properly. Even if the connector pins are not damaged, the pins mating with and disconnecting from the backplane will cause the system to interpret a board failure. Using the ejectors ensures that the board connector mates with the backplane in one continuous movement.
- Using the handle to insert or remove an interface processor, or failing to push the ejectors to the full 90-degree position, can leave some (not all) of the connector pins mated to the backplane, a state which will hang the system. Using the ejectors and making sure that they are pushed fully into position ensures that all three layers of pins are mated with (or free from) the backplane.

It is also important to use the ejector levers when removing an interface processor to ensure that the interface processor bus connector pins disconnect from the backplane in the logical sequence expected by the system. Any interface processor that is only partially connected to the backplane can hang the bus. For detailed steps on how to perform OIR, refer to the section “Installing and Configuring Processor Modules” in the chapter “Maintaining the Router.”

Figure 1-22 Ejector Levers and Captive Installation Screws



Microcode

The Cisco 7505 supports downloadable microcode for most upgrades, which enables you to load new microcode images into Flash memory.

The latest microcode version for each interface processor type is bundled with the system software image. New microcode images are now distributed on floppy disk as part of a software maintenance release; microcode upgrades are no longer distributed individually.

The default operation is to load the microcode from the bundled image. At system startup, an internal system utility scans for compatibility problems between the installed interface processor types and the bundled microcode images, then decompresses the images into running memory (DRAM). The bundled microcode images then function the same as images loaded from the individual microcode ROMs on the processor modules.

Note The software and interface processor microcode images are carefully optimized and bundled to work together. Overriding the bundle can result in incompatibility between the various interface processors in the system.

Caution To ensure proper operation of the system and to avoid system problems, you should use *only* the microcode images that are bundled.

To instruct the system to boot a microcode image other than the default at startup, use the **microcode** *interface-type* [**system** | **flash** | **rom**] **filename** configuration command to add the instructions to the configuration file. The **system** option tells the system to load from the system bundle. All processors of the same type (for example, all FIPs) will load the same microcode image, either from the default source or from the source you specify.

The **show microcode** command lists all of the microcode images that are bundled with the system software image. In order to support OIR, the system loads a microcode image for all available processor types. Following is an example of the **show microcode** command. (The indicated versions and descriptions are intended as examples only.)

```
Router# show microcode
Microcode bundled in system

Card    Microcode    Target Hardware    Description
Type    Version      Version
----    ---------    ---------------    -----------
EIP      10.1              1.x          EIP version 10.1
FIP      10.2              2.x          FIP version 10.2
TRIP     10.1              1.x          TRIP version 10.1
AIP      10.5              1.x          AIP version 10.5
FSIP     10.6              1.x          FSIP version 10.6
FEIP     10.1              1.x          FEIP version 10.1
HIP      10.2              1.x          HIP version 10.2
MIP      11.0              1.x          MIP version 11.0
CIP      10.3              1.x          CIP version 10.3

Router#
```

The microcode version and description lists the bundled microcode version for each processor type, which is not necessarily the version that is currently loaded and running in the system. A microcode image loaded from ROM or a Flash memory file is not shown in this display. To display the currently loaded and running microcode version for each processor, use the **show controller cybus** command.

The target hardware version lists the minimum hardware revision required to ensure compatibility with the new software and microcode images. When you load and boot from a new bundled image, the system checks the hardware version of each processor module that it finds installed and compares the actual version to its target list. If the target hardware version is different from the actual hardware version, a warning message appears when you boot the router, indicating that there is a disparity between the target hardware and the actual hardware. You will still be able to load the new image, however, contact a service representative for information about upgrades and future compatibility requirements.

To display the current microcode version for each interface processor, enter the **show controller cybus** command. The following example shows that an FSIP is running Microcode Version 1.0:

```
Router# show cont cybus

  (display text omitted)
 FSIP 0, hardware version 4, microcode version 1.0
  (display text omitted)
```

Although most microcode upgrades are distributed on floppy disk, some exceptions may require EPROM replacement. If so, refer to the chapter "Maintaining the Router," for replacement procedures. Instructions are also provided with the upgrade kit. For complete command descriptions and instructions, refer to the related software documentation.

Environmental Monitoring and Reporting Functions

The environmental monitoring (ENVM) and reporting functions, on the chassis interface board, enable you to maintain normal system operation by identifying and resolving adverse conditions prior to loss of operation. Environmental monitoring functions constantly monitor the internal chassis air temperature and DC line voltages. The power supply monitors its own voltage and temperature and shuts itself down if it detects a critical condition within the power supply. If conditions reach shutdown thresholds, the system shuts down to avoid equipment damage from excessive heat or current. The reporting functions periodically log the values of measured parameters so that you can retrieve them for analysis later, and the reporting functions display warnings on the console if any of the monitored parameters exceed defined thresholds.

In addition to monitoring internal temperature and voltage levels, the system also monitors the fan array. If any one or more of the fans fail, the system displays a warning message on the console. If the fan is still not operating properly after two minutes, the system shuts down to protect the internal components against damage from excessive heat.

Environmental Monitoring

The environmental monitoring functions use the following levels of status conditions to monitor the system. The processor uses the first four levels to monitor the temperature inside the processor slots, and the power supply uses the Normal and Critical levels to monitor DC voltages. Table 1-4 lists temperature thresholds for the first four (processor-monitored) levels. Table 1-5 lists the DC power thresholds for the Normal and Critical (power-supply-monitored) levels.

- Normal—All monitored parameters are within normal tolerances. The fans operate at 55 percent of their maximum speed if the internal air temperature does not exceed this level.
- Warning—The system is approaching an out-of-tolerance condition. The system will continue to operate, but operator monitoring or action is recommended to bring the system back to a normal state. If the internal air temperature reaches 23 C (73 F), the fan speed will increase linearly from 55 percent of maximum speed until it reaches 100 percent speed at 33 C (91 F).

- Critical—An out-of-tolerance temperature or voltage condition exists. The system may not continue operation. If a voltage measurement reaches this level, the power supply can shut down the system. If a fan in the fan array fails, the system will display a warning message and shut down in two minutes. Immediate operator action is required.
- Processor shutdown—The processor has detected a temperature or fan-failure condition that could result in physical damage to system components and has disabled all DC power. Immediate operator action is required. Before shutdown, the system logs the status of monitored parameters in NVRAM so that you can retrieve it later to help determine the cause of the problem. The system power remains off until the operator toggles the system power switch off and on again.
- Power supply shutdown—The power supply has detected an out-of-tolerance voltage, current, or temperature condition within the power supply and has shut down (or a shutdown is imminent). All DC power remains disabled until the operator toggles the AC power and corrects the problem that caused the shutdown (if any). This condition is typically because of one of the following reasons:
  - Loss of AC or DC input power (the AC or DC source failed)
  - Power supply detected an overvoltage, overcurrent, AC or DC undervoltage, or overtemperature condition within the power supply (this includes operator shutdown by turning off the system power switch, which the power supply interprets as an undervoltage condition).
- Fan failure — One or more of the fans has failed. This message is displayed for two minutes, after which the system initiates a full processor shutdown.

Table 1-4 Processor-Monitored Temperature Thresholds

Parameter	Warning	Normal	Warning	Critical	Shutdown
Inlet air	< 10 C	10–39 C	39–46 C	46–64 C	> 64 C
Airflow	< 10 C	10–70 C	70–77 C	77–88 C	> 88 C

Table 1-5 Power-Supply Monitored Voltage Thresholds

Parameter	Critical	Normal	Critical
+5V	< 4.74V	4.74–5.26V	> 5.26V
+12V	< 10.20V	10.20 to 13.8V	> 13.80V
-12V	> –10.20V	–10.20 to –13.80V	< –13.80V
+24V	< 20.00V	20.00 to 28.00V	> 28.00V

The system uses the first four status levels (Normal, Warning, Critical, and Processor Shutdown) to monitor the air temperature in the interface processor compartment and the voltage levels on the four DC lines. Sensors on the chassis interface monitor the temperature of the cooling air that flows through the processor slots. If the air temperature exceeds a defined threshold, the system processor displays warning messages on the console terminal and, if the temperature exceeds the shutdown threshold, it shuts down the system. The system stores the present parameter measurements for both temperature and DC voltage in NVRAM, so that you can retrieve it later as a report of the last shutdown parameters.

The power supply self-monitors its own internal temperature and voltages. The power supply is either within tolerance (Normal) or out of tolerance (Critical level), as shown in Table 1-5. If an internal power supply temperature or voltage reaches a critical level, the power supply shuts down without any interaction with the system processor.

If the system detects that AC or DC input power is dropping, but it is able to recover before the power supply shuts down, it logs the event as an intermittent powerfail. The reporting functions display the cumulative number of intermittent powerfails logged since the last power up.

Environmental Reports

The system displays warning messages on the console if chassis interface-monitored parameters exceed a desired threshold or if a fan failure occurs. You can also retrieve and display environmental status reports with the **show environment**, **show environment all**, **show environment last** and **show environment table** commands. Parameters are measured and reporting functions are updated every 60 seconds. A brief description of each of these commands follows. For complete command descriptions and instructions, refer to the related software documentation.

Caution To prevent overheating the chassis, ensure that your system is drawing cool inlet air. Overtemperature conditions can occur if the system is drawing in the exhaust air of other equipment. When viewing the chassis from the interface processor end, the airflow inlet vents are on the right side of the chassis, and the exhaust vents are on the left. (See Figure 1-5.) Ensure adequate clearance around the sides of the chassis so that cooling air can flow through the chassis interior unimpeded. Obstructing or blocking the chassis sides will restrict the airflow and can cause the internal chassis temperature to exceed acceptable limits.

The **show environment** command display reports the current environmental status of the system. The report displays the date and time of the query, the refresh times, the overall system status, and any parameters that are out of the normal values. No parameters are displayed if the system status is normal. The example that follows shows the display for a system in which all monitored parameters are within Normal range.

```
Router# show env

Environmental Statistics
  Environmental status as of Wed 5-10-1995 16:42:48
  Data is 0 second(s) old, refresh in 60 second(s)

  All Environmental Measurements are within specifications
```

If the environmental status is *not* normal, the system reports the worst-case status level in the last line of the display, instead of the status summary that is shown in the last line of the preceding example.

The **show environment last** command retrieves and displays the NVRAM log of the reason for the last shutdown and the environmental status at that time. If no status is available, it displays the reason as *unknown*.

```
Router# show env last

Environmental Statistics
  Environmental status as of Wed 5-10-1995 16:42:48
  Data is 10 second(s) old, refresh in 50 second(s)

  All Environmental Measurements are within specifications

LAST Environmental Statistics
  Environmental status as of Wed 5-10-1995 12:22:43
  Power Supply: 600W, OFF

  No Intermittent Powerfails

  +12 volts measured at  12.05(V)
   +5 volts measured at   4.82(V)
  -12 volts measured at -12.00(V)
  +24 volts measured at  23.90(V)

  Air-Flow temperature measured at 32(C)
  Inlet    temperature measured at 26(C)
```

The **show environment table** command displays the temperature and voltage thresholds for each monitored status level, which are the same as those listed in Tables 1-4 and 1-5. The current measured values are displayed with the unit of measure noted, (V) or (C), and each is listed below a column heading that indicates its current status level. Measurements that fall within the Normal range are displayed in the Normal column of the table, while measurements that have reached a critical level are shifted to the Critical column, and so on.

In the following example, all current measured values fall within the Normal status range. The first voltage parameter in the table, +12(V), shows that the Normal range for the +12V sense spans 10.20V through 13.80V. The current measured value, 12.05V, falls within that range and is therefore displayed in the Normal column.

```
Router# show env table
Environmental Statistics
  Environmental status as of Wed 5-10-1995 18:50:21
  Data is 46 second(s) old, refresh in 14 second(s)

  WARNING: Fan has reached CRITICAL level

Voltage Parameters:

 SENSE        CRITICAL               NORMAL               CRITICAL
-------|--------------------|------------------------|--------------------

+12(V)                   10.20      12.05(V)      13.80
 +5(V)                    4.74       4.96(V)       5.76
-12(V)                  -10.20     -12.05(V)     -13.80
+24(V)                   20.00      23.80(V)      28.00

Temperature Parameters:

SENSE     WARNING       NORMAL       WARNING       CRITICAL      SHUTDOWN
------|------------|------------|------------|-------------|------------

Inlet              10   32(C)   39            46             64
Air-flow           10   40(C)   70            77             88
```

The following example shows only the Temperature Parameters section of the table. In this example, the measured value at the inlet sensor is 41 C, which falls within the warning range (39 C through 46 C) and therefore is displayed in the Warning column.

```
Temperature Parameters:

SENSE     WARNING       NORMAL       WARNING       CRITICAL      SHUTDOWN
------|------------|------------|-------------|--------------|------------

Inlet               10           39    41(C)   46             64
Air-flow            10   40(C)   70            77             88
```

The **show environment all** command displays an extended report that includes all the information in the **show environment** command display, plus the power supply status, the number of intermittent powerfails (if any) since the system was last powered on, and the measured values at the temperature sensors and the DC lines. The refresh time indicates that the parameters will be measured again in 29 seconds; any changes to a measurement will not be reflected in the display until at least 40 seconds have elapsed and the current information is refreshed.

```
Router# show env all
Environmental Statistics
  Environmental status as of Wed 5-10-1995 19:10:41
  Data is 31 second(s) old, refresh in 29 second(s)

  WARNING: Fan has reached CRITICAL level
  Power Supply: 600W AC (or 600W DC)
  No Intermittent Powerfails

  +12 volts measured at  12.00(V)
   +5 volts measured at   5.02(V)
  -12 volts measured at -12.05(V)
  +24 volts measured at  23.70(V)

  Airflow temperature measured at 35(C)
  Inlet   temperature measured at 26(C)
```

Fan Shutdown

When the system power is on, all six fans in the fan array must be operational. If the system detects a failed or failing fan, it will display a warning message on the console screen. If the condition is not corrected within two minutes, the entire system will shut down to avoid an overtemperature condition and possible damage.

The system uses a Hall Effect signal to monitor the six fans in the array. The current to the fans and the magnetic field generated by the fans' rotation generates a voltage, which the system monitors to determine whether or not all of the fans are operating. If the monitored voltage signal drops below a specified value, the system assumes a fan failure and initiates a fan shutdown.

In the following example, the system has detected an out-of-tolerance fan, which it interprets as a fan failure. The failure message is displayed for two minutes before the system shuts down.

```
%ENVM-2-FAN: Fan array has failed, shutdown in 2 minutes
```

If the system does shut down because of a fan failure, the system will display the following message on the console screen and in the environment display when the system restarts:

```
Queued messages:
%ENVM-1-SHUTDOWN: Environmental Monitor initiated shutdown
```

For complete command descriptions and instructions, refer to the related software command reference documentation, which is available on UniverCD or in print.